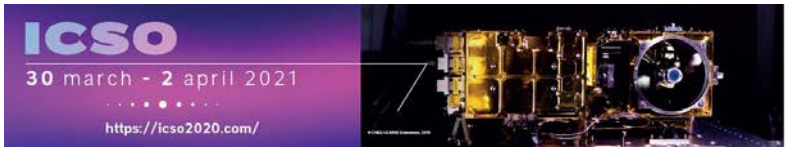
International Conference on Space Optics—ICSO 2020

Virtual Conference

30 March–2 April 2021

Edited by Bruno Cugny, Zoran Sodnik, and Nikos Karafolas



Design of a true HDR, backside illuminated image sensor with charge domain binning

International Conference on Space Optics — ICSO 2020, edited by Bruno Cugny, Zoran Sodnik, Nikos Karafolas, Proc. of SPIE Vol. 11852, 1185215 · © 2021 ESA and CNES
CCC code: 0277-786X/21/$21 · doi: 10.1117/12.2599226

Design of a true HDR, backside illuminated image sensor with charge domain binning

Dierickx B., Kalgi A.K, Sezgin B., Oblan S., Liekens K., Salinas I.,

Caeleste, Mechelen, Belgium

ABSTRACT

The ELFIS2 image sensor has a unique combination of properties, being true high dynamic range (HDR), charge domain global shutter (GS), backside illumination (BSI) and a TID and SE hard design. It is stitchable to a resolution of n*1k by m*1k pixels on a 15µm pitch.

Keywords: image sensor, radiation hard, backside illumination, stitching, high dynamic range, global shutter

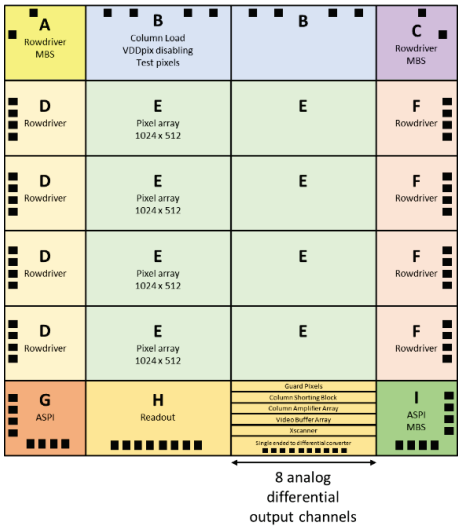
1. INTRODUCTION

ELFIS [1-3] was the first image sensor that had a unique combination of properties, being true HDR (high dynamic range), true global shutter, of both types integrate-while-read (IWR) and integrate-then-read (ITR), backside illumination and design for TID hardness. It had a resolution 1920x1080 pixels on a 15µm pitch.

In this paper we describe its successor, which has the same pixel size and topology and the same key features as HDR, BSI, global shutter and TID hardness.
It features following improvements
→ A lower read noise, and thus a proportionally higher dynamic range as the Q_{FW} will remain the same.
→ Stitchability from 1k x 0.5k pixels up to waferscale or 9k x 9k pixels
→ It has an experimental charge domain binning method
→ Improved SEU- and SET-hardness
We will at the moment of the conference have completed the design. A detailed specification prediction can be given, yet there will be no measured performance data.

2. FLOORPLAN AND SPECIFICATIONS

The ELFIS2 is a fully "stitchable" version of the ELFIS1[1-3]. The unit block is as large as 1k x 0.5k pixels. The baseline device that will be manufactured measures 2k x 2k pixels. Specifications per default apply to this size.



←Figure 1 is top level floorplan of the ELFIS2, represented as "stitch blocks". Key part of the array are lithographically printed using the stitch unit blocks numbered "A" to "I".

Pixels are arranged per 1024x512 pixels of an "E" block. Row drivers providing the controls for pixel switches are present in D and F blocks.
The B block contains column biasing and pixel supply connections.
The H block contains the X-multiplexing and the 8-channel readout structure.
A, C, G, I are the corner blocks containing register upload and other housekeeping parts.

←Figure 1: Stitching configuration of the ELFIS2 sensor

Specifications shortlist

Pixel pitch	15 um
illumination	Backside illumination (BSI) EPI thickness up to 22 µm
Shutter	Charge domain global shutter
Target read noise at nominal speed Target read noise in "low noise mode"	< 4e- in high gain mode < 2e- in high gain mode
Full well charge (Q_{FW})	10ke- in high gain mode 160ke- in low gain mode, global shutter IWR 320ke- in low gain mode, global shutter ITR
High dynamic range	By off-chip combination of the high gain and low gain responses. Reaching values from 92 dB in nominal mode, global shutter IWR To 104dB in low noise mode, global shutter ITR
Pixel rate per channel	40 MHz pixel frequency
Number of output channels	8 Analog differential outputs per stitch block (per 1024 pixels in X)
Frame rate	140 fps for 2k x 2k resolution, single pass
Off chip companion ADC	Companion 12-bit (nominal mode) ADC implemented outside the sensor area to be assembled on PCB
PLS	>200:1
Binning	2x2 Charge domain binning
Back biasing	Design is backbias compatible.
Color filter	No color filters, yet color-filter compatible.
Radhardness	Fully radhard design: TID >> 50kRad, SEL > LET 60 MeV.cm^2/mg

3. PIXEL DESIGN

The ELFIS2 pixel is a direct successor of the ELFIS pixel[3]. Its schematic circuit is shown in Figure 2.

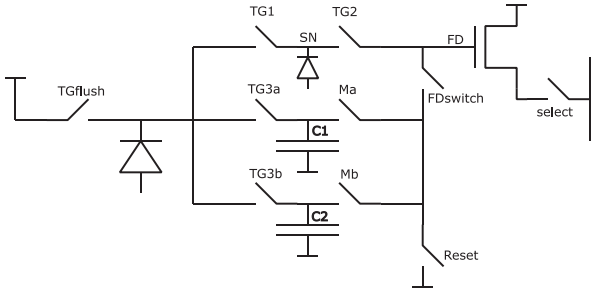


Figure 2: Schematic representation of the pixel

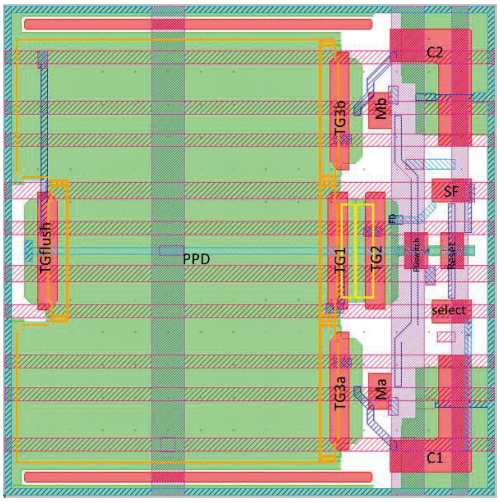


Figure 3: Layout of the pixel with only active and poly layers shown

4. HDR OPERATION

The high dynamic range is obtained by converting the photocharge of a given integration time to a voltage (signal) twice. The first charge to voltage conversion is on a small capacitance, resulting in a "high gain" (HG) signal S1, the second conversion is on a large capacitance leading to low gain (LG) signal S2. Effectively one has two Q_{FW}.

1. Low Q_{FW} (high gain): $Q_{FW} \approx 10000e$-
2. High Q_{FW} (low gain) in ITR mode of operation: $Q_{FW} \approx 320000$ e-

The low Q_{FW} uses the "classic" Storage Node (SN) of the Global Shutter (GS) CMOS technology.
The high Q_{FW} uses overflow capacitors to store an amount of charge that exceeds the charge storage of the SN.
In order to realize IWR (integrate while read) two sets of high Q_{FW} capacitors are used, on which the charge is stored for odd and even frames.

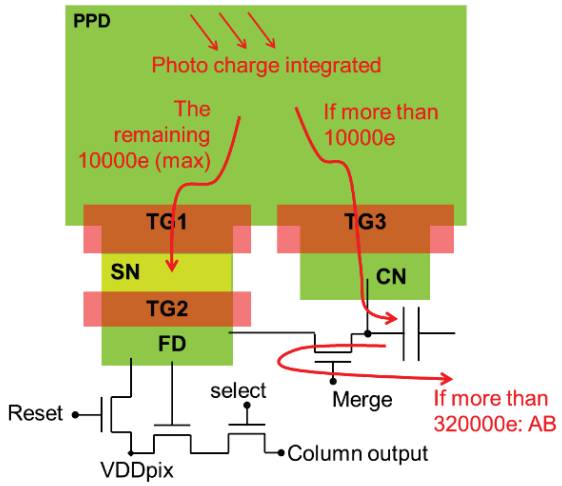


Figure 4: operation of the HDR pixel during charge integration. The first 10000 electrons are integrated in the PPD and stored in the SN.

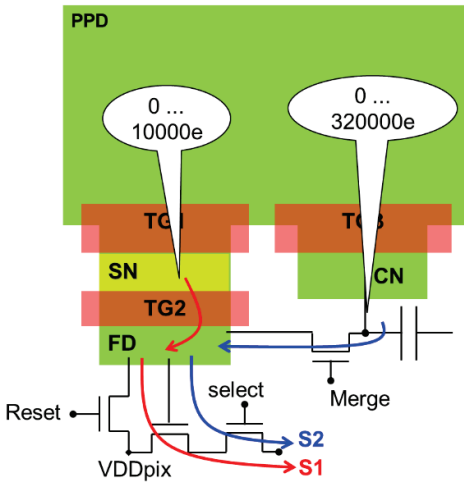


Figure 5: Operation of the HDR pixels at readout time. S1 is the high gain signal, with small Q_{FW}, S2 is the low gain signal, with large Q_{FW}.

During the integration time photo-electrons are accumulated in the pinned photodiode (PPD) (Figure 4). If the amount of electrons in the PPD exceeds ~10000, these overflow over TG3 into the capacitor node (CN), for later use. There are two CNs with a total capacity for 320000 electrons. If the total charge exceeds even this 320000 electrons, it overflows to the anti-blooming drain. At the end of the integration time, the (maximally) 10000 electrons still present in the PPD are transferred by transfer gate TG1 to the storage node (SN).

Just before the moment of readout, there are thus

- Between 0 and 10000 electrons in the storage node (SN)
- Between 0 and 320000 on the CN (= C1 + C2)

The total integrated photocharge is the sum of those two.

At the moment of readout (Figure 5) TG2 is toggled and transfers the photocharge charge from SN to the floating diffusion (FD), where is it read out using correlated double sampling (CDS), yielding a signal "S1". Immediately afterwards the switch "Merge" is closed, shunting the FD and the CN (C1, C2). The sum of both charge packets is on FD, and is read out, yielding a signal "S2"

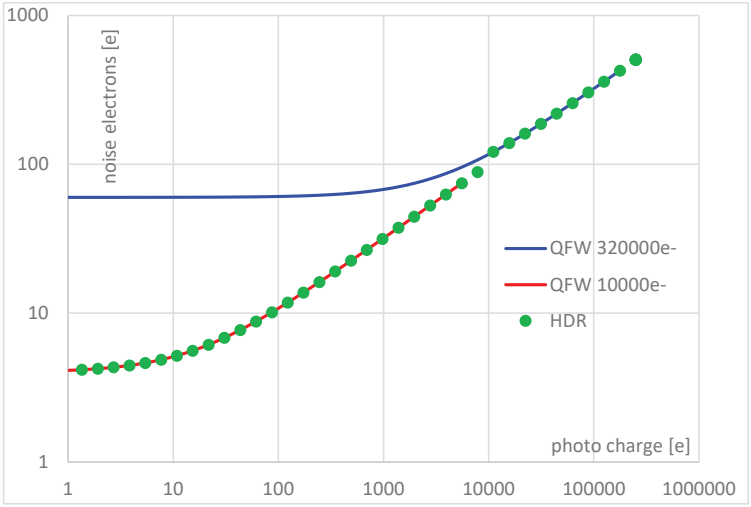


Figure 6: Noise (Y-axis) versus signal (X-axis) of the ELFIS2, in nominal mode high gain and low gain, and in the "HDR" combination of both.

At each illumination level both low Q_{FW} and high Q_{FW} signals are measured. The "HDR" signal is a combination of these. The combined dynamic range is defined as {max Q_{FW}} / {min Q_{noise}}

The predicted dynamic range is then:

DR defined as {max Q_{FW}} / {min Q_{noise}}	DR in high gain	DR in low gain	Combined (H)DR
Nominal mode, global shutter IWR	10000/4 ≈ 2500:1	160000/30 ≈ 5000:1	160000/4 ≈ 40000:1 = 92dB
Low noise mode, global shutter ITR	10000/2 ≈ 5000:1	320000/60 ≈ 5000:1	320000/2 ≈ 160000:1 = 104dB

HDR interpolation algorithm

The ELFIS2 outputs per pixel two signals, S1 and S2.

As one normally needs to express the photoresponse of a pixel as a single numeric value, S1 and S2 must be off-chip combined. On our set-up we use the following algorithm to combine the signals HG (S1) and LG (S2) into a single HDR value.

In a first step, both the S1 and S2 signals are separately FPN and PRNU corrected.

Then the S1 and S2 signals are scaled with a factor so that both signals coincide in the valid range of S1.

Then for each pixel we consider the value of S1:
If the HG "S1" signal is above 75% of S1 saturation
→take the LG signal S2
When the HG signal is below 50% of S1 saturation
→ take the HG value S1
Between 50% and 75%:
→ apply a weighted interpolation between S1 (HG) and S2 (LG) as shown in Figure 7

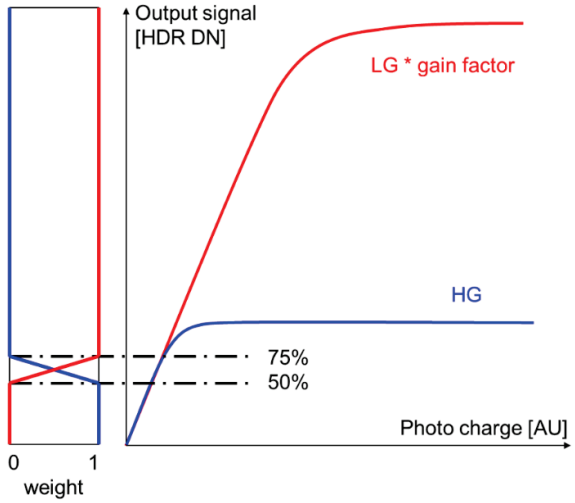


Figure 7: Weighted interpolation between HG and LG signals

5. CHARGE DOMAIN BINNING

In the context of image sensors, binning is the readout of the information of the image sensor, whereby the signals of a group of pixels are summed or averaged and read out as a single "binned" signal.

There are many different methods to realize binning, with following coarse classification:

1. "Charge domain" binning, where all photo charges of the group of pixels are added together, and then as a whole converted to a voltage. Such is straightforward in CCDs and it can also be done in certain types of "shared" CMOS pixels.
2. "Voltage domain" binning, whereby the voltage output signals of the group of pixels are averaged on-chip to an average voltage signal. Many embodiments exist here as well.
3. Digital domain binning, whereby the binning operation happens in digital domain, after image acquisition and AD conversion.

The advantages of binning are

→ Faster, lower power, readout of an imager, exchanging speed or power for resolution.
→ In case of "charge domain binning" one has the additional benefit of increase of sensitivity [V.m²/W.s] and noise equivalent flux. This advantage is not reached with voltage domain binning and digital domain binning.

The ELFIS2 uses a novel way to do charge domain binning in regular CMOS pixels.

One operates or biases the pixels in the pixel array differently. Certain pixels are operated normally to have "charge collecting photodiodes" or "charge collecting junctions", others are operated so that they are *not* or *less* charge collecting.
In order to be *not* or *less* collecting, the non-collecting junctions must be at an intermediate potential, higher than the junction being forward biased towards the substrate, yet lower than the bias of the collecting junctions.
This is realized by letting the non-collecting pixels or their photodiode "float" (not being forced at a potential) or explicitly biased at a suitable lower potential.

It is beneficial that the depletion layer of the collecting junctions extends widely and overlaps between the neighboring junctions. Widely extending depletion layers imply the use of high resistivity material. However, it is possible to reach the effect as well in normal resistivity material.
Having a thick high resistivity material as compared to the pixels size is thus beneficial. With a pixel size (pixel pitch) of 15µm, the layer thickness must be in the order of 10µm or more.
The method works best in backside illuminated configuration, yet also in frontside illuminated image sensors the method can work.

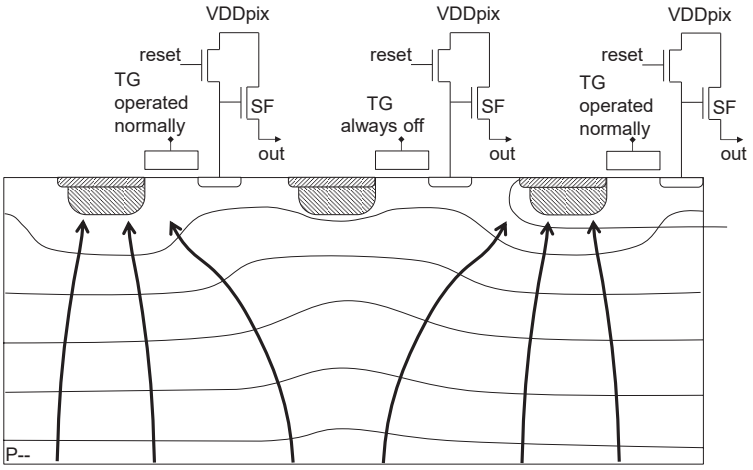


Figure 8: cross sections of three pixels, showing the ELFIS2 concept of charge domain binning.

In the example of Figure 8 three neighboring 4T pixels are shown schematically. The two outer pixels are operated to be charge collecting, the middle pixel is operated to be not collecting. The photodiode is made floating by permanently turning off the transfer gate TG. As the photodiode has no path to drain the photocurrent, its potential will drop to the level that the PPD-substrate diode becomes forwards biased, or that the TG leaks.

6. READOUT CHAIN

Figure 9 show the analog signal chain from pixels to bondpad.

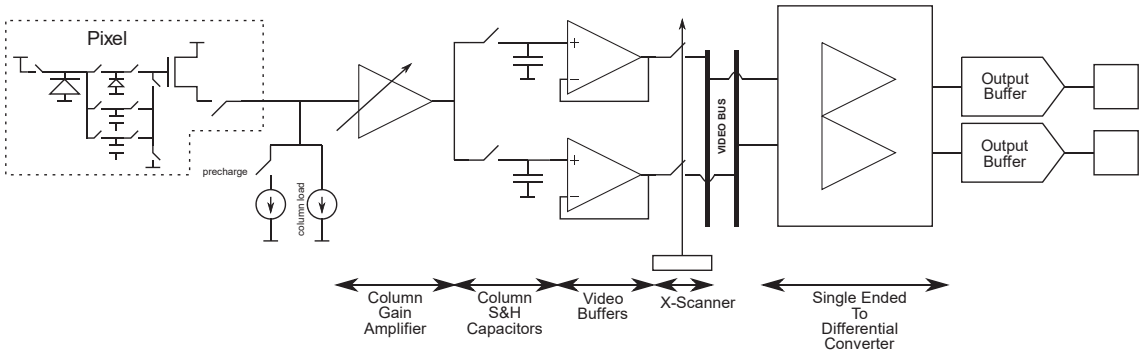


Figure 9: Simplified analog chain

The output of in-pixel source follower is buffered or amplified by a programmable gain amplifier. The reset and signal values of the pixel are sampled separately to execute correlated double sampling (CDS) down the chain. The sampled

voltages are buffered onto the video bus through video buffers. The single ended to differential (S2D) converter serves to convert the native pseudo differential signal to fully differential signals. The output of all the single ended to differential converters are multiplexed at pixel output frequency and buffered to the output.

The readout chain contains various options to program gain, to reduce the read noise, and to perform fixed pattern noise cancellation, not shown for simplification.

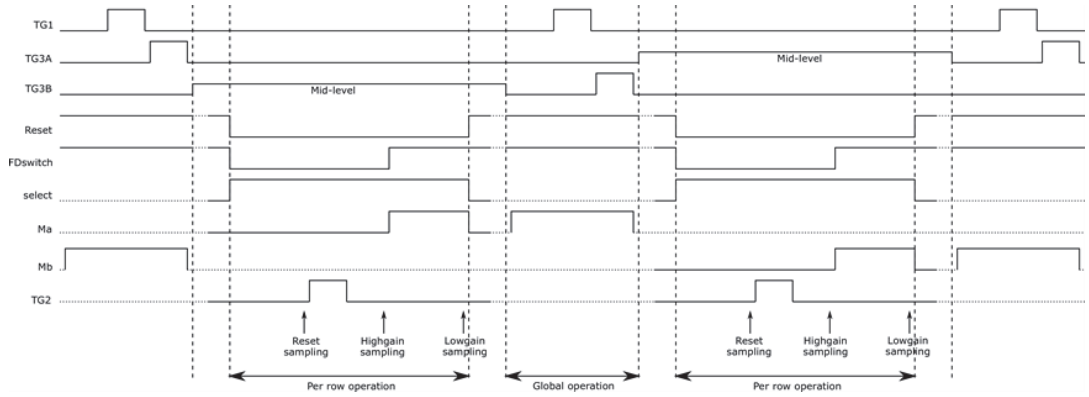


Figure 10: Typical global shutter timing

The overall timing diagram of the sensor (Figure 10) can be grouped into 2 operation regions.

- Global operations

These operations are performed on the whole sensor. It includes transfer of charges from PPD to SN. Additionally, any remaining charges on PPD are fully transferred onto the low gain capacitor by toggling the transfer gate that was biased at mid-level in the previous readout cycle. PPD and the low gain capacitor (readout from previous readout cycle) are reset before the readout begins.

- Per row operations

The readout is performed per row. A pixel row is addressed for readout. The reset level of FD, high gain signal level after the charge transfer and low gain signal level after the merge operation are all sampled onto the S&H capacitor. The high gain and low gain signals are sampled sequentially and readout out in the same order. CDS is executed only on the high gain signal, for the low gain signal a DC reference is used.

ACKNOWLEDGMENTS

The ELFIS2 sensor is developed as part of ESA contract 4000133295 [2].
We acknowledge the fruitful collaborations with the ESA/ESTEC staff (Noordwijk, NL), Airbus Defense & Space (Toulouse, FR), LFoundry S.r.l. (Avezzano, IT).

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