Advance TEM application in 10 nm and below technology node chips

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ABSTRACT

In 10nm and below technology node, the device changes smaller and introduced some new process changes, some advance TEM methods are used in the 10nm and below device process monitor or research tools during the process developing. We did some advance TEM research on Fin and metal gate, and some examples are given in this paper. It is clearly show the importance of advance TEM method play essential role in process monitor and process developing.

Keywords: TEM application, fin structure, dummy gate

1. INTRODUCTION

In 10nm and below technology node, the device change smaller and introduced some new process changes, such as Fin structure and CD, with the addition of strain engineering, the Fin stress changed. Some advance TEM methods are used in the 10nm and below device process monitor or research tools during the process developing. Some example are given in this paper. It is clear show the importance of advance TEM methods play a vital role in process monitor and process developing.

2. THE STUDY OF FIN

2.1 Structure and fin

At 10nm and below technology node, there are multi-Vt devices in logic and core device area. The Fin CD will introduce the sub-Vt effect, so that there are Fin treatment process for improvement the Fin profile to reduce the Fin CD even results reduce the sub-Vt effect.

The FinFET is 3D structure devices, the normal top-down CD SEM cannot perform the 3D measurement for Fin structure. The precision cross-section TEM is used to do the 3D measurement for Fin structure. For 300mm wafer, the photo pattern/etch, CMP and Iso/dense micro-loading etch-effect may affect the Fin profile in wafer different locations. we need good control all these effects to get same Fin structure in same wafer different location (such as chips location in wafer center, donut and edge, same chip pattern iso and dense area) and different wafer same locations. In order to reduce operation effect, the FEI wafer level FIB tool is best for this application.

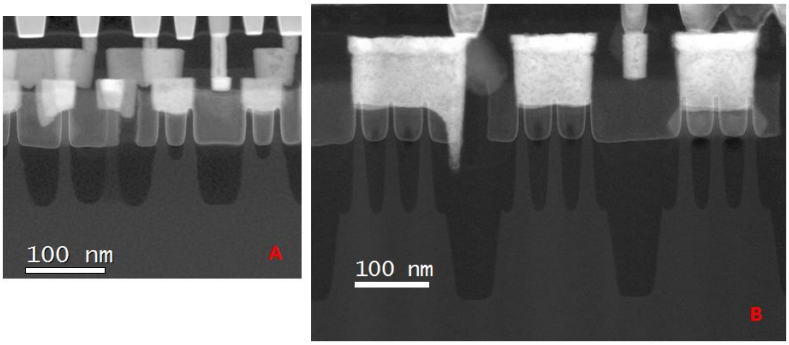

Figure 1. The STEM images of 10nm chips.

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We used advance TEM methods to research the 10nm chips of the two companies, as shown in Figure 1(Figure 1). The part A is from A company while part B is from B company. The images show that the two company chips with almost same metal gate height, but the B company Fin CD is much narrow than A company and the B company sub-Fin height is much higher than A company. There is deep trench isolation for the different transistor in B company chip, so that the latch-up perform may be better.

The normal TEM is design for materials study, it is not special design for CD measurement. For IC industrial CD measurement, the dimensional measurement error is less than 1% for different magnification and different tools. The normal TEM only can control below 5%. but not for all magnifications. So that the TEM for these CD measurement need special selected and perform special measurement before ship-out in vendor site. The TEM need weekly perform calibration, and all measurement images must be taken under control defocus region.

2.2 Strain measurement

In FinFET structure, e-SiGe is used for stress engineering of channel. The e-SiGe epitaxy grown needs to provide lower DIBL and higher stress effect for short channel device. The TEM base channel strain measurement was used to speed up the etch and epitaxy schemed of e-SiGe. The TEM base strain measurement method including the following[1]: NBD (nano-beam diffrction)[2-3], HRTEM GPA[4], CBED (Converge beam electron diffraction)[5-6], Electron beam Holography[7-8], and PED (Precession electron diffraction)[9-11]. Due to bigger tilted specimen angle from normal [110] or [100] directions for CBED method, The CBED method is not used in device channel strain measurement. The HRTEM GPA method, the high quality HRTEM need very thin TEM specimen, the free surface introduce strain relaxed affect this method used in strain measurement in 65-40-28nm plane-devices. But for FinFET device, the Fin structure is less than 20nm, the field of view and specimen drifting are the limited for this method. For strain measurement, the Si substrate without strain is used as reference site.

For 10nm device, the following methods can be used: NBD, PED, Electron beam Holography, SMF (scanning morie fringes)[12-13] and HRSTEM GPA. For below 10nm FinFET, due to the Fin structure change to more narrow and higher, after S/D e-SiGe epitaxy grown, there are small angle tilted at Fin channel area comparing with Si substrate, as is shown in Figure 2(Figure 2). So that the following method cannot be used in 7nm and below technology node for TEM base channel strain analysis: Electron beam Holography, SMF (scanning morie fringes) and HRSTEM GPA.

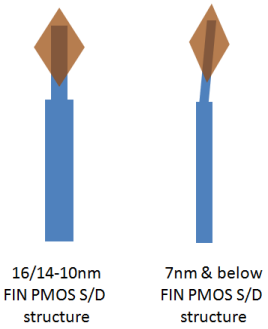

Figure 2. The Fin and S/D SiGe epitaxy structure.

3. THE DUMMY GATE AMORPHOUS SI LAYER CRYSTAL GRAIN STUDY

In 10nm and below technology node, the SADP lithography method is used for gate pattern/etch. SiN spacer deposition need go through high temperature process, so that some amorphous Si may change to nano or polycrystalline, which may increase the line edge roughness of dummy gate. the gate line edge roughness may affect the wafer yield and gate to contact TDDB test results.

After dummy gate pattern/etch, the dummy gate need go through the SiN/SiCN spacer deposition, N/P S/D epitaxy grown, SiN etch stop layer deposition. All these thermal-process may results the polycrystalline grains formed in dummy gate, the Si(111) oriental crystal grains would difficult etch during RGP(replace gate process) results poly-remaining and affect the transistor Vt perform.

The PED method can be used to study the amorphous Si layer can pass the thermal process highest temperature limited without nano-or polycrystalline grains form so that can set process margin for the process before gate pattern/etch or before RPG process.

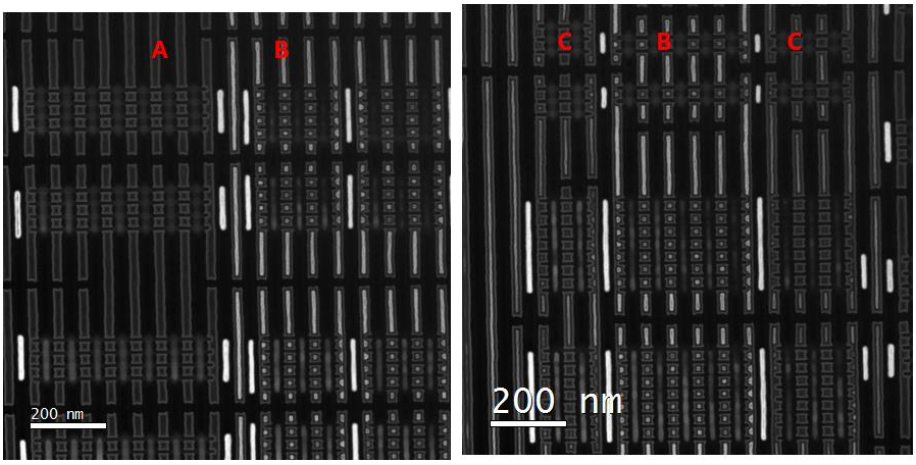

Figure 3. The plane view STEM images of A company 10nm chip. Based on the metal gate filling condition, there are three different Vt transistors in the STEM imaging area, there are marked as type A, B and C.

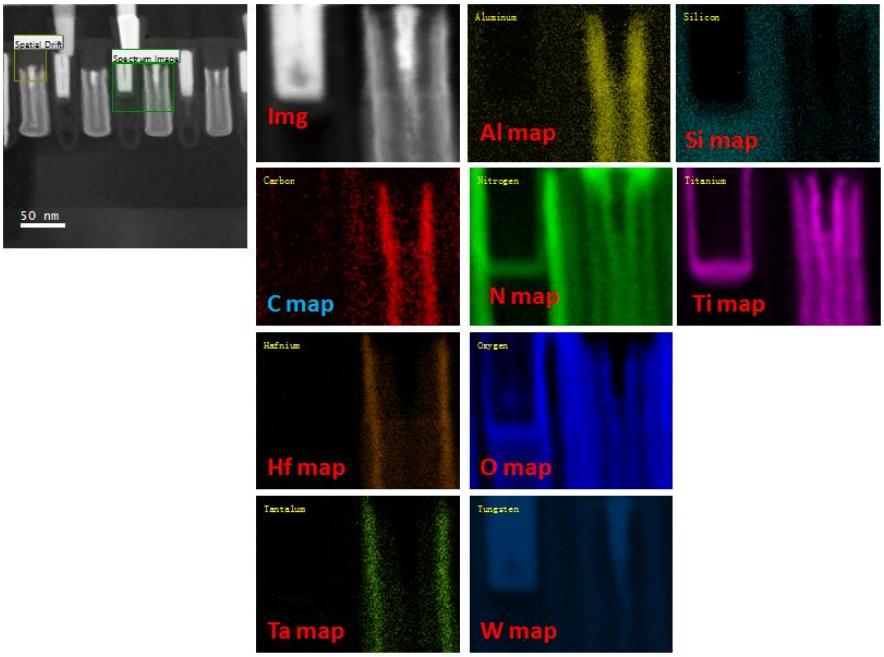

Figure 4. The STEM and EELC mapping of the A company metal gate. The different elements in the metal gate structure are shown.

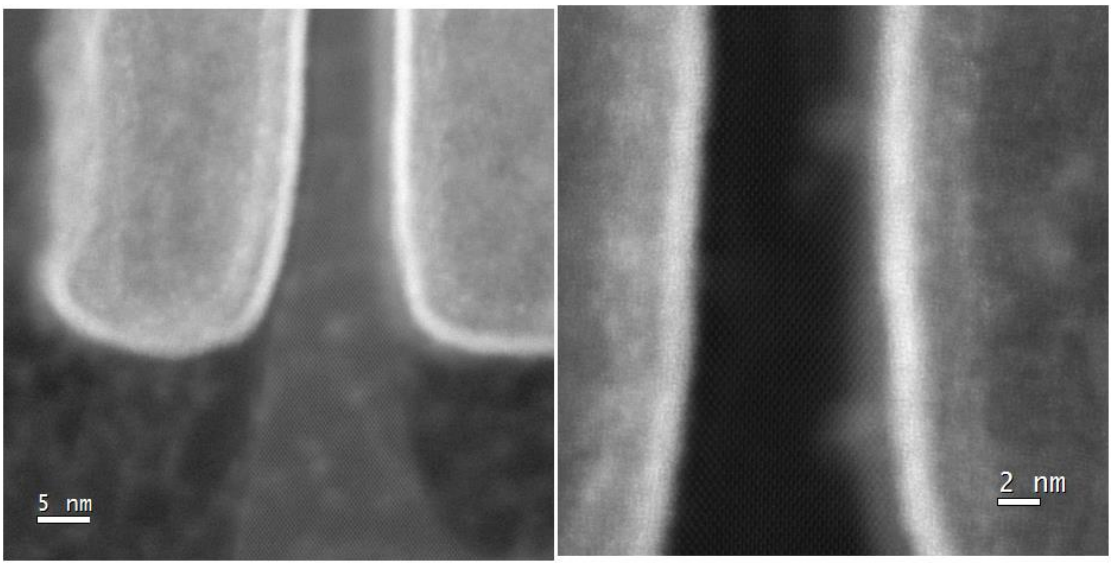

Figure 5. The HRSTEM images of Fin and HK/MG structures.

In 10nm and below technology node, the multi-Vt design need perform the gate metal pattern/etch process, for NMOS low Vt or ultra-low Vt transistor, the TaN barrier layer need remove, so that it is easy dry etch damage the HfOx layer at Fin top result the gate leakage. So that it is need to check the HfOx layer thickness and possible crystalline on the Fin. In normal TEM mode, the HRTEM mode need focus the e-beam on the interest area result e-beam heat effect and HfOx may change to polycrystalline or other artifact. The HRSTEM is best method to study the HfOx layer thickness and poly-crystalline. HRSTEM combine EELS mapping can provide both structure and chemical information with high spatial resolution.

4. CONCLUSION

In 10nm and below technology node, the device change smaller and introduced some new process changes. As an effective tools, the advance TEM methods can provide many help in 10nm and below technology node chip process monitor and process developing stage.

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