

PROCEEDINGS OF SPIE

***Photonics Packaging, Integration,  
and Interconnects VIII***

**Alexei L. Glebov**

**Ray T. Chen**

*Editors*

**22–24 January 2008**

**San Jose, California, USA**

*Sponsored and Published by*

SPIE

**Volume 6899**

Proceedings of SPIE, 0277-786X, v. 6899

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Author(s), "Title of Paper," in *Photonics Packaging, Integration, and Interconnects VIII*, edited by Alexei L. Glebov, Ray T. Chen, Proceedings of SPIE Vol. 6899 (SPIE, Bellingham, WA, 2008) Article CID Number.

ISSN 0277-786X  
ISBN 9780819470744

Published by

**SPIE**

P.O. Box 10, Bellingham, Washington 98227-0010 USA  
Telephone +1 360 676 3290 (Pacific Time) · Fax +1 360 647 1445  
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# Er<sub>x</sub>Y<sub>2-x</sub>SiO<sub>5</sub> nanocrystal and thin film for high gain per length material

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## ABSTRACT

We report on fabricating Er<sub>x</sub>Y<sub>2-x</sub>SiO<sub>5</sub> nanocrystals using ErCl<sub>3</sub>·6H<sub>2</sub>O and YCl<sub>3</sub>·6H<sub>2</sub>O solutions and Si nanowires grown by VSL method. Use of crystalline host allows incorporation of up to 25 at. % Er without clustering and loss of optical activity, and use of Y enables continuous mixing of Er and Y for controlling cooperative upconversion. We obtain a cooperative upconversion coefficients of  $(2.2 \pm 1.1) \times 10^{-18}$  cm<sup>3</sup>/s and  $(5.4 \pm 2.7) \times 10^{-18}$  cm<sup>3</sup>/s at an Er concentration of  $1.2 \times 10^{21}$  cm<sup>-3</sup> and  $2.0 \times 10^{21}$  cm<sup>-3</sup>, respectively. These values are up to 10 times lower at 10 times higher Er concentration than those reported for Er-doped silica, and shows that up to 69 dB/cm gain could be achieved for ultra-compact optical amplification. Also, we report on the deposition of Er<sub>x</sub>Y<sub>2-x</sub>SiO<sub>5</sub> thin film on Si substrate using ion beam sputter deposition. Rapid thermal annealing at 1100 °C is enough to form crystal phase the film and activate most of Er<sup>3+</sup> ions.

**Keywords:** erbium, silicate, upconversion, Si photonics

## 1. INTRODUCTION

There is a strong and growing interest in developing Si-photonics that can integrate the fast, loss-less information carrying capacity of photonics with Si integrated circuit technology to overcome the impending “interconnect bottleneck”.<sup>1,2</sup> In particular, a great effort has been made in developing a Si-based light source, especially a laser, that can overcome the inherent limitation of the indirect bandgap of Si. Among the many possible ways of obtaining light emission from Si using the rare earth ion Er<sup>3+</sup> as an optical dopant has attracted a special attention because of its ability to provide light at 1.5 μm that is compatible not only with optical telecommunication but also with silicon-on-insulator based Si microphotonic devices. Furthermore, Er-doping has a history of proven success in providing optical gain and lasing when doped into silica fiber amplifiers (EDFA).<sup>3</sup>

The intra-4f transition of Er<sup>3+</sup> that gives rise to the 1.5 μm luminescence is parity-forbidden, and occurs due to the effects of the crystal field surrounding Er<sup>3+</sup> ions. This leads to long luminescence lifetimes and, when doped into an amorphous host such as silica, large inhomogeneous broadening of the atomic luminescence peak that allow for low-noise, broad-band amplification capability of EDFAs. Unfortunately, the same qualities can lead to severe limitations for its applicability for Si photonics that requires a large optical gain in a limited wavelength range from a micrometer-sized volume, since the combination of long luminescence lifetimes and a broad luminescence peak results in a low gain cross section at a particular wavelength. Increasing the gain requires a very high Er concentration, but the concentration of optically active Er that can be doped into a host material without clustering is limited, even for an amorphous host such as silica. Another way of increasing the gain cross section per wavelength is reducing the inhomogeneous broadening of Er<sup>3+</sup> luminescence by using a crystalline host matrix, but even in that case, controlling the location of Er<sup>3+</sup> ions down to atomic levels is difficult.<sup>4</sup>

A rather interesting alternative to Er-doping that can overcome these difficulties is to raise the Er concentration high that a stable, Er-rich crystalline phase can form. In particular, crystalline rare-earth oxyorthosilicates (R<sub>2</sub>SiO<sub>5</sub>) provide a combination of a very high concentration of optically active rare earth ions in a stable material. Furthermore, since there are only 2 possible sites for rare earth ions<sup>5</sup> that are separated by either oxygen atoms or SiO<sub>4</sub> tetrahedra, the rare earth ions are expected to suffer very little inhomogeneous broadening, as well as be dispersed on an atomic scale as

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not to suffer from clustering or segregation. Indeed, there have been many reports of using various combination of  $R_2SiO_5$  to realize efficient solid-state lasers.<sup>6</sup>

Such lasers, however, used bulk crystals grown from a crucible, and therefore are not compatible with integrated photonics that require materials in a thin-film form. We report on producing single-phase  $Er_xY_{2-x}SiO_5$  nanocrystal aggregates on a large scale using  $ErCl_3 \cdot 6H_2O$  and  $YCl_3 \cdot 6H_2O$  dissolved ethanol solution and Si nanowire (Si-NW) arrays as templates and  $Er_xY_{2-x}SiO_5$  thin film on Si substrate using ion beam sputter deposition. Analysis shows that while cooperative upconversion occurs at high Er concentrations, the cooperative upconversion coefficient of fabricated  $Er_xY_{2-x}SiO_5$  nanocrystal is only  $(2.2 \pm 1.1) \times 10^{-18} \text{ cm}^3/\text{s}$  and  $(5.4 \pm 2.7) \times 10^{-18} \text{ cm}^3/\text{s}$  at an Er concentration of  $1.2 \times 10^{21} \text{ cm}^{-3}$  and  $2.0 \times 10^{21} \text{ cm}^{-3}$ , respectively. Also, the X-ray diffraction and photoluminescence spectra of  $Er_xY_{2-x}SiO_5$  thin film shows the rapid thermal annealing at 1100 °C is enough to crystallize the thin film indicating that a viability of this material to make efficient, high-gain Si based optical device for Si photonics.

## 2. EXPERIMENT

### 2.1 Fabrication of $Er_xY_{2-x}SiO_5$ nanocrystals

Figure 1 shows the SEM images representing fabrication process of  $Er_xY_{2-x}SiO_5$  nanocrystal aggregates. (a) Vertically aligned single crystalline Si-NWs were grown by vapor-liquid-solid mechanism using Au catalyst deposited on Si (111) substrates by sputtering. During growth,  $SiCl_4$  was introduced into growth furnace held at 900 °C by bubbling  $H_2$  carrier gas through liquid  $SiCl_4$  held at 0 °C at a flow rate of 1~10 sccm. Ar and  $H_2$  gas was also introduced into the furnace at a flow rate of 100 sccm, respectively. The growth time was 30 min. (b) After Si-NW growth, an Er and Y solution prepared by dissolving  $ErCl_3 \cdot 6H_2O$  and  $YCl_3 \cdot 6H_2O$  into ethanol was spin coated on the Si-NW. (c) Following spin-coating, a rapid thermal anneal at 900 °C for 4 min in a flowing  $N_2/O_2$  environment followed by another anneal at 1200 °C for 3 or 5 min in a flowing Ar. The Si-NWs provide large surface area for chemical reaction and atomic transport between Si, Er, and Y. And by varying the ratio of  $ErCl_3 \cdot 6H_2O$  and  $YCl_3 \cdot 6H_2O$  solutions, the composition of the final nanocrystal could be varied from pure  $Y_2SiO_5$  to pure  $Er_2SiO_5$ . The intended Er concentrations which could be controlled by varying the Er/Y ratio, were 0 (i.e., pure  $Y_2SiO_5$ ), 0.26, 1, 2, 5, 10, 18, and 25 at. % (i.e., pure  $Er_2SiO_5$ ). These values, except for the 0.26 at. % due to the detection limit, were confirmed by energy-dispersive x-ray spectroscopy (EDS) to be 1.5, 2.5, 5, 8.8, 17, and 25 at. %. EDS measurement was performed at three different points for each sample and averaged. For avoiding error from Si substrate, the ratio of Er and Y were fitted for EDS.

### 2.2 Deposition of $Er_xY_{2-x}SiO_5$ thin film

We use ion beam sputter deposition system to make thin film of  $Er_xY_{2-x}SiO_5$ . The thin films were grown on Si substrate with the target of Y (99.9 %) and Er (99.9 %) chips attached on Si wafer under  $O_2$  gas flow. By varying the number of attached Y and Er chips and  $O_2$  gas flow rate we can control the composition of deposited film. The base pressure was  $\sim 5 \times 10^{-7}$  torr, and the ion energy was 600 eV. The compositions of deposited films were analyzed with Rutherford backscattering spectroscopy. The compositions of as-deposited films are  $Er_{0.02}Y_{1.9}SiO_{5.0}$ ,  $Er_{0.18}Y_{1.7}SiO_{4.6}$ , corresponding Er concentrations of 0.26, and 2.4 at. %, respectively, and the thickness of the films is about 160 nm. After the deposition, the films were rapid thermal annealed at various temperatures in a flowing  $O_2$  environment to optically activate  $Er^{3+}$  ions.

The structure of the resulting silicate nanocrystal and film was analyzed using x-ray diffraction (XRD). Photoluminescence (PL) spectra were measured using an Ar laser (488 nm) or frequency doubled  $YVO_4:Nd$  laser (532 nm), monochromator, a thermoelectrically cooled InGaAs detector, and the standard lock-in technique.

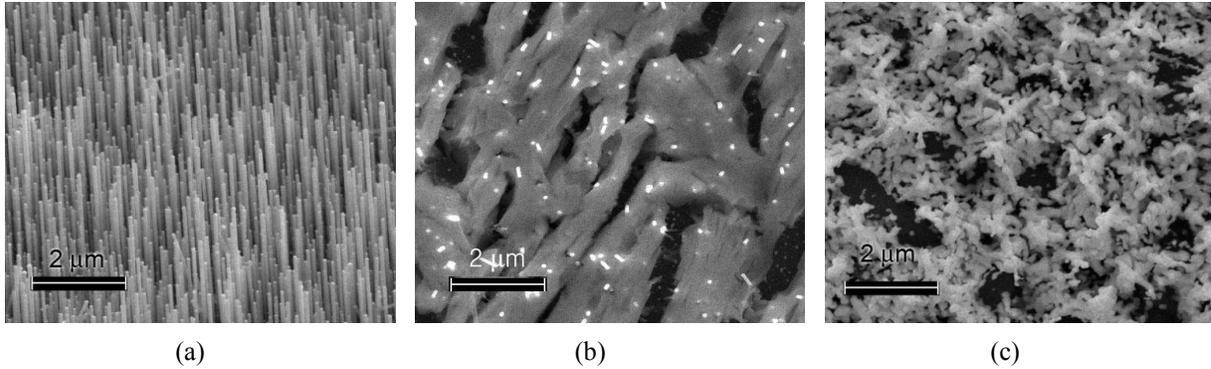


Figure 1. The typical SEM images showing fabrication process of  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  nanocrystal aggregates. (a) Vertically aligned Si-NWs were grown on Si (111) substrate. (b)  $\text{ErCl}_3 \cdot 6\text{H}_2\text{O}$  and  $\text{YCl}_3 \cdot 6\text{H}_2\text{O}$  dissolved solution was spin coated on Si-NWs. (c) Rapid thermal annealing at 900 °C for 4 min in a flowing  $\text{N}_2/\text{O}_2$  environment and then at 1200 °C for 3 or 5 min in a flowing Ar environment.

### 3. RESULTS AND DISCUSSION

#### 3.1 $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$ nanocrystal aggregates

Figure 2 (a) shows the  $2\theta$  x-ray diffraction spectra ( $28\sim 29^\circ$ ) of fabricated nanocrystal aggregates with various Er concentrations. It shows the identical spectra of all samples ranging from pure  $\text{Y}_2\text{SiO}_5$  (i.e. 0 at. %) to pure  $\text{Er}_2\text{SiO}_5$  (i.e. 25 at. %) and also the peak positions agree well with the reference from JCPDS which is represented by open ( $\text{Y}_2\text{SiO}_5$ , #52-1809) and closed circle ( $\text{Er}_2\text{SiO}_5$ , #52-1810).  $\text{Er}_2\text{SiO}_5$  and  $\text{Y}_2\text{SiO}_5$  have same crystal structure and nearly identical lattice constant. Figure 2 (b) shows the PL spectra of fabricated nanocrystal aggregates, normalized to the intensity at 1.53  $\mu\text{m}$ . The PL spectra are also nearly identical irrespective of composition. The intra-4f transitions of  $\text{Er}^{3+}$  are parity forbidden but partially allowed by the crystal field and therefore  $\text{Er}^{3+}$  PL spectra indirectly represent the local atomic environment of Er. It suggests that the crystal structure is the same for all samples, right down to atomic level. No 980 nm luminescence were observed for low Er concentrations even though we excite Er to higher-lying level indicating that thermal relaxation down to the first excited level is very rapid. This is consistent with the high phonon energy of rare-earth silicates,  $1000\text{ cm}^{-1}$ .<sup>7</sup> The fast thermal relaxation of  $^4\text{I}_{11/2}$  level shows the viability of 980 nm pump. However, note that 980 nm luminescence for Er concentration of 5 at. % or higher were observed, even the pump power was the same.

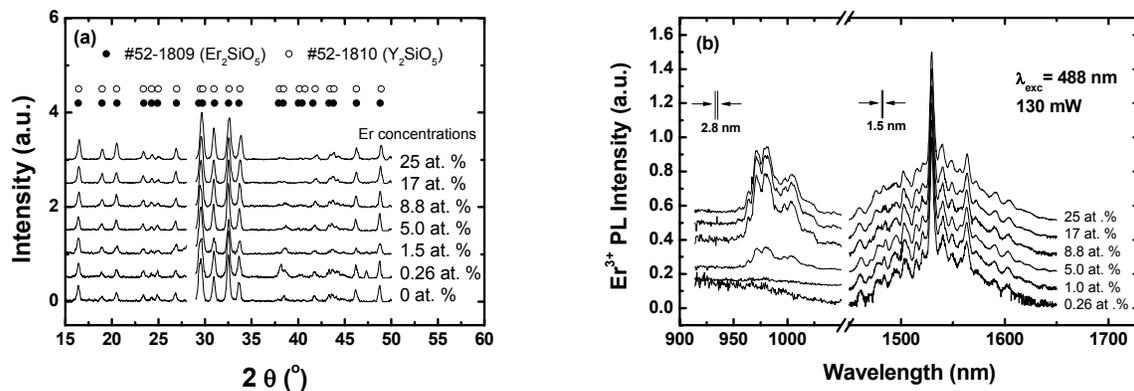


Figure 2. (a) X-ray diffraction and (b) photoluminescence spectra of the fabricated nanocrystal aggregates. Nearly identical spectra indicate that the crystal structure of the fabricated nanocrystal is the same for all samples, right down to atomic level.

Figure 3 shows the decay traces of 1.53  $\mu\text{m}$   $\text{Er}^{3+}$  PL intensity of the sample with 1.5 at. % Er as the pump power was increased from 2 mW to 353 mW. As the pump power is increased, the decay traces become non-exponential with shorter lifetimes. We note, however, that all decay traces, after the fast, initial decay, approach a single exponential decay. Such pump-power dependent 1.53  $\mu\text{m}$   $\text{Er}^{3+}$  PL decay traces indicate cooperative upconversion, in which an  $\text{Er}^{3+}$  ion in the first excited state ( $^4\text{I}_{13/2}$ ) decays non-radiatively to the ground state ( $^4\text{I}_{15/2}$ ) by exciting another  $\text{Er}^{3+}$  ion in the first excited state to the third excited state ( $^4\text{I}_{9/2}$ ), which then thermalizes rapidly to lower-lying states (either to  $^4\text{I}_{11/2}$  state, which can result in 0.98  $\mu\text{m}$  emission, or back to  $^4\text{I}_{13/2}$  state). This is an important loss mechanism that limits optical gain in  $\text{Er}^{3+}$  based 1.53  $\mu\text{m}$  amplifiers and lasers, and must be investigated if  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  is to be used for optical amplifiers.

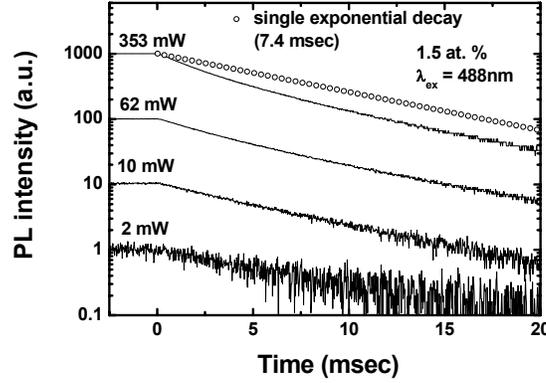


Figure 3. Pump power dependent luminescence decay curve of the fabricated nanocrystal aggregates with 1.5 at. % Er.

### 3.2 Cooperative upconversion coefficient of $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$ nanocrystal aggregates

To investigate the cooperative upconversion coefficient we assumed the 2-level model in which we consider the ground and first excited states of  $\text{Er}^{3+}$  only. This is based on the fast thermal relaxation. Although  $\text{Er}^{3+}$  ions are pumped to  $^4\text{F}_{7/2}$  or  $^4\text{S}_{3/2}$  state, it decays to the first excited state,  $^4\text{I}_{13/2}$ , with the time scale of  $\sim 10$   $\mu\text{sec}$  by thermal relaxation. In such a case, we can write the rate equation of the first excited state like Eq. (1) where,  $n$ ,  $\sigma$ ,  $\phi$ ,  $\tau$ ,  $C$ ,  $N$  is fraction of  $\text{Er}^{3+}$  in the first excited state, the excitation cross section, pump photon flux, decay lifetime without cooperative upconversion, cooperative upconversion coefficient, and concentration of Er, respectively. The Eq. (2) and Eq.(3) are the analytic solutions of rate equation.  $n(t)$  is the time dependent fraction of first excited state when the pump is off and  $n(0)$  is the first excited state fraction of the steady state at the pump photon flux of  $\phi$ .

$$\frac{dn(t)}{dt} = \sigma\phi(1-n) - \frac{n}{\tau} - CNn^2 \quad (1)$$

$$n(t) = \frac{1}{\tau} \left[ \left( \frac{1}{\tau n(0)} + CN \right) \exp(t/\tau) - CN \right]^{-1} \quad (2)$$

$$n(0) = \frac{\sigma\phi + 1/\tau}{2CN} \left\{ \left[ 1 + \frac{4CN\sigma\phi}{(\sigma\phi + 1/\tau)^2} \right]^{1/2} - 1 \right\} \quad (3)$$

Cooperative upconversion coefficients can be obtained by fitting these equations with pump power dependence of 1.53  $\mu\text{m}$  PL intensity and decay curve simultaneously, provided that  $\sigma$  and  $\tau$  are known. We use the value of  $\sigma$  and  $\tau$  from the sample with 0.26 at. % Er whose cooperative upconversion is negligible. The excitation cross section  $\sigma$  was obtained from the risetime measurement as a function of pump photon flux and is  $(4.5 \pm 2.3) \times 10^{-20}$   $\text{cm}^2$  at the pump wavelength of 488 nm and  $(2.3 \pm 1.2) \times 10^{-20}$   $\text{cm}^2$  at the pump wavelength of 532 nm. This value is an order of magnitude higher than the typical value. We attribute this large excitation cross section to multiple scattering of pump photon by nanocrystal aggregates. To confirm this, the sample with 0.26 at. % Er was spin-coated with PMMA to reduce the difference of refractive index between nanocrystal and surroundings. The refractive index of  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  is about 1.7

and that of PMMA is 1.48. After PMMA coating, the excitation cross section of the sample with 0.26 at. % Er was decreased 26 %. The decay lifetime without cooperative upconversion,  $\tau$ , was also obtained from the sample with 0.26 at. % Er, 7.4 msec.

Figure 4 shows the pump power dependent PL intensity and decay traces of Er concentration 1.5 and 2.5 at. % at the pump wavelength of 532 nm. By using a single set of parameters to fit both curves using Eq. (2) and Eq. (3), we obtained cooperative coefficients of  $(2.2 \pm 1.1) \times 10^{-18} \text{ cm}^3/\text{sec}$  and  $(5.4 \pm 2.7) \times 10^{-18} \text{ cm}^3/\text{sec}$  at 1.5 at. % and 2.5 at. %, respectively. The fitting result of  $C = 1.5 \times 10^{-18} \text{ cm}^3/\text{s}$  with  $n(0) = 0.086$  for 1.5 at. % and  $C = 4.2 \times 10^{-18} \text{ cm}^3/\text{s}$  with  $n(0) = 0.049$  for 2.5 at. % ( $\sigma = 2.3 \times 10^{-20} \text{ cm}^2$ ) is shown by solid curve in figure 4. These values are relatively small compared to Er doped silica in considering the Er concentrations and comparable to Er doped soda-lime silicate. In case of Er doped silica, C was reported to be as high as  $1.7 \times 10^{-17} \text{ cm}^3/\text{s}$  at an Er concentration of  $1 \times 10^{20} \text{ cm}^{-3}$ .<sup>8</sup> A better result was reported for bulk soda-lime silicate glasses whose C was  $1.2 \times 10^{-18} \text{ cm}^3/\text{s}$  at an Er concentration of  $6 \times 10^{20} \text{ cm}^{-3}$ .<sup>9</sup> Note, however, that the glasses prepared from batches melted at 1400 °C for as long as 50 hrs.

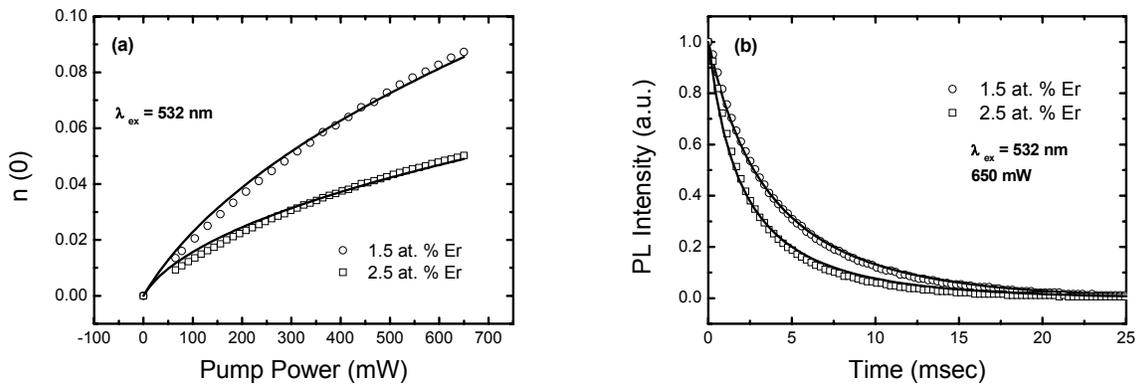


Figure 4. (a) The  $1.53 \mu\text{m}$   $\text{Er}^{3+}$  PL intensity as a function of pump power and (b) the decay traces at the pump power of 650 mW from the sample with 1.5 at. % (circle) and 2.5 at. % (square) Er at the pump wavelength of 532 nm. By using a single set of parameters to fit both curves with Eqs. (2) and (3) when  $\sigma = 2.3 \times 10^{-20} \text{ cm}^2$  is used, we obtain values of  $C = 1.5 \times 10^{-18} \text{ cm}^3/\text{s}$  and  $n(0) = 0.086$  and  $C = 4.2 \times 10^{-18} \text{ cm}^3/\text{s}$  and  $n(0) = 0.049$ . The fitting results are shown as the solid curves.

### 3.3 Inversion curve

Figure 5 shows the inversion curve of the fabricated  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  nanocrystal aggregates with 1.5 and 2.5 at. % Er calculated using 2-level assumption and obtained cooperative upconversion coefficient. Here we assume that the pump wavelength is 1480 nm, the  $\text{Er}^{3+}$  absorption cross section is  $3 \times 10^{-21} \text{ cm}^2$  at 1480 nm and  $\text{Er}^{3+}$  emission cross section is  $1 \times 10^{-20} \text{ cm}^2$  at 1530 nm. For 1.5 at. % Er, population inversion can be achieved at a pump intensity of  $52 \text{ kW}/\text{cm}^2$ , and 42 dB/cm gain, corresponding to 90% inversion, can be achieved at a pump intensity of  $800 \text{ kW}/\text{cm}^2$ . The maximum possible gain for 2.5 at. % Er is as high as 69 dB/cm, corresponding to 90 % inversion, at the pump intensity of  $3.1 \text{ MW}/\text{cm}^2$ . In fact, because there must be a process that can reduce the efficiency such as excited state absorption, the real pump intensity that is needed to invert population is higher than the calculated value.

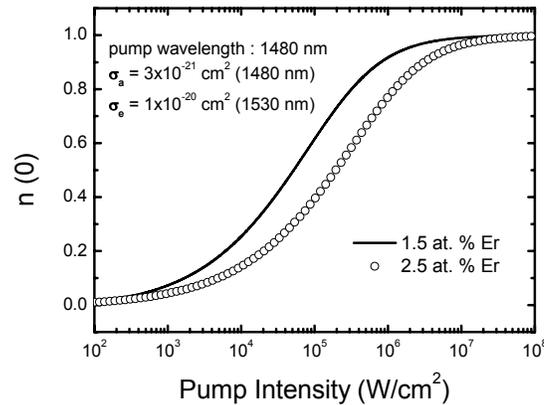


Figure 5. The inversion curve of the fabricated  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  nanocrystal aggregates with 1.5 and 2.5 at. % Er calculated using 2-level assumption and obtained cooperative upconversion coefficient. Here we assume that the pump wavelength is 1480 nm, the  $\text{Er}^{3+}$  absorption cross section is  $3 \times 10^{-21} \text{ cm}^2$  at 1480 nm and  $\text{Er}^{3+}$  emission cross section is  $1 \times 10^{-20} \text{ cm}^2$  at 1530 nm.

### 3.4 $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$ thin film

Figure 6 shows the XRD spectrum of the deposited film which is rapid thermal annealed at 1100 °C in flowing  $\text{O}_2$  environment for 20 min. The peak positions agree well with reference from JCPDS which is shown by vertical line and no other crystal phases could be observed indicating that the film has  $\text{Y}_2\text{SiO}_5$  crystal phase dominantly. However, it has to be investigated whether the film has small amount of residual amorphous phase (such as  $\text{SiO}_2$ ) or another crystal phases (such as  $\text{Y}_2\text{O}_3$ ,  $\text{Y}_2\text{Si}_2\text{O}_7$ ) which can be scattering center in the film.

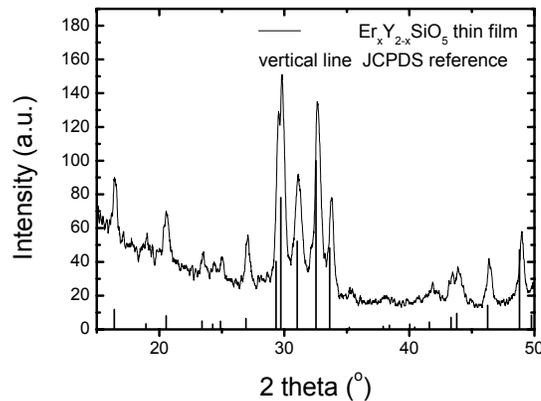


Figure 6. X-ray diffraction spectrum of the deposited  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  thin film which is rapid thermal annealed at 1100 °C in flowing  $\text{O}_2$  environment for 20 min. The peak positions agree well with reference from JCPDS which is shown by vertical line.

Figure 7 (a) shows the PL spectra of the deposited films normalized to intensity at 1.53  $\mu\text{m}$ . For comparison, the PL spectrum of the  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  nanocrystal aggregates (1.5 at. %) is also shown. Curves are offset for clarity. By contrast with the film rapid thermal annealed at 900 °C showing broad PL spectra within system resolution, the films rapid thermal annealed at 1100 or 1200 °C show sharp peaks similar to that of the  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  nanocrystal aggregates. The positions of main (1530 nm) and sub peaks of thin film rapid thermal annealed above 1100 °C agree well with nanocrystal aggregates indicating that similar atomic structure of  $\text{Er}^{3+}$  in  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  nanocrystal and thin film. Figure 7

(b) shows the  $\text{Er}^{3+}$  PL peak intensity and decay lifetime of the deposited film with 2.4 at. % Er at various annealing conditions. Dramatic changes of the  $\text{Er}^{3+}$  PL peak intensity and decay lifetime can be seen after rapid thermal annealing above 1100 °C. The increase of PL peak intensity is accompanied with decay lifetime indicating that increase of PL peak intensity result from the increase of luminescence efficiency of  $\text{Er}^{3+}$ . In comparison with rapid thermal annealing at 1100°C for 3 min, the higher temperature or the longer annealing time result in about 10 % PL intensity increase with little changes in decay lifetime. It indicates that although further annealing of the film can give additional  $\text{Er}^{3+}$  activation, it may be very low fraction. Therefore, for deposited thin film, rapid thermal annealing at 1100 °C in flowing  $\text{O}_2$  for 3 min is enough to form  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  crystal phase and activate most of  $\text{Er}^{3+}$  ions. In case of the fabrication of  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  nanocrystal aggregates, 1200 °C annealing is necessary to form crystal phase.

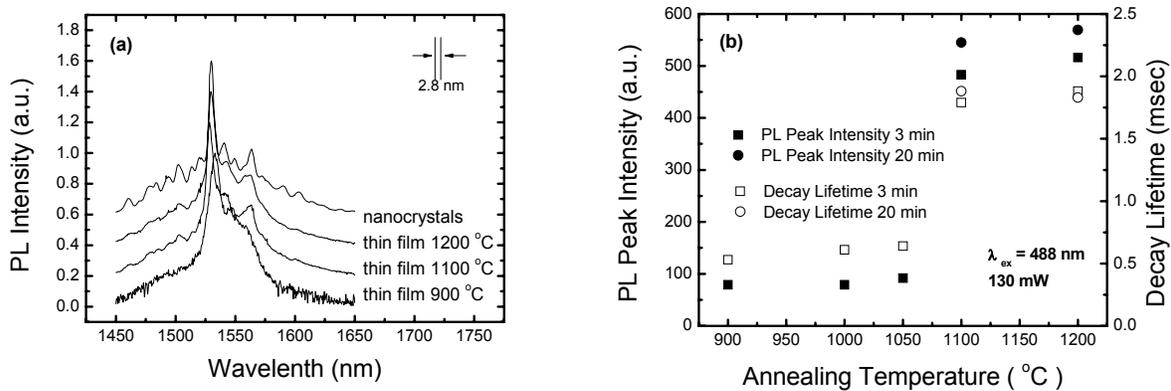


Figure 7. (a)  $\text{Er}^{3+}$  photoluminescence (PL) spectra of the deposited  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  thin films with 2.4 at. % Er normalized to intensity at  $1.53\mu\text{m}$ . For comparison, the PL spectrum of the  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  nanocrystal aggregates (1.5 at. %) is also shown. Curves are offset for clarity. (b)  $\text{Er}^{3+}$  PL peak intensity (closed) and decay lifetime (open) of the deposited  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  thin films as a function of rapid thermal annealing temperature. The films were rapid thermal annealed for 3 min (square) or 20 min (circle).

#### 4. CONCLUSION

In conclusion, we have investigated  $\text{Er}^{3+}$  luminescence in  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  nanocrystal aggregates fabricated using Si nanowires and thin film deposited by ion beam sputter deposition. Analysis of the  $\text{Er}^{3+}$  PL intensity and decay time shows that the cooperative upconversion coefficient of  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  nanocrystal aggregates is only  $(2.2\pm 1.1)\times 10^{-18} \text{ cm}^3/\text{s}$  and  $(5.4\pm 2.7)\times 10^{-18} \text{ cm}^3/\text{s}$  at an Er concentration of  $1.2\times 10^{21} \text{ cm}^{-3}$  and  $2.0\times 10^{21} \text{ cm}^{-3}$ , respectively. This is nearly 10 times lower at 10 times higher Er concentration than that reported from Er-doped silica. Rapid thermal annealing at 1100 °C for 3 min of  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  thin film is enough to form  $\text{Er}_x\text{Y}_{2-x}\text{SiO}_5$  crystal phase and activate most of  $\text{Er}^{3+}$  ions.

#### ACKNOWLEDGMENT

This work was supported in part by NRL and by grant No. (R11-2003-022) from OPERA of the Korea Science and Engineering Foundation.

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# Comparison of Bandwidth Limits for On-card Electrical and Optical Interconnects for 100 Gb/s and Beyond

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## ABSTRACT

Aggregate chip bandwidths in server and high performance computing have exceeded Tb/s, and if present trends are to continue would lead to doubling the number of signal pins in each generation. For high bandwidth switch and server applications, bandwidth requirements could exceed the package pin limit as early as 2012.

We defined metrics to compare the performance of electrical and optical interconnects, which includes bandwidth density (Gb/s/mm<sup>2</sup>/port), media bandwidth\*distance product (GHz\*m), power consumption (mW/Gb/s/Port), and technology comparison metric (Gb/s/mm<sup>2</sup>/port \* GHz\*m/mW/Port). We will show that optical interconnects offer a performance metric improvement factor of greater than 25 over electrical interconnects.

**Keywords:** Optical interconnects, Electrical interconnects

## 1. INTRODUCTION

Bandwidth demands in server and high performance computing environments have been increasing at least as fast as Moore's law, with aggregate chip bandwidths exceeding Tb/s. Because electrical signaling rates are reaching practical equalization limits, there will soon be a need to double the number of signal pins in each generation if present trends are to continue. For high bandwidth switch and server applications, bandwidth requirements could exceed the package pin limit as early as 2012. This has lead many companies to evaluate and develop strategies to transition to optical interconnect technologies which offer the potential of higher bandwidth density, lower power consumption and scalability. The most promising technologies at present are parallel solutions using VCSEL and receiver arrays and polymer waveguides as a transmission medium. To determine the limits of interconnect technologies, we have defined appropriate metrics, computed them and compared the performance of electrical and optical interconnects. The metrics includes the bandwidth density (Gb/s/mm<sup>2</sup>/port), media bandwidth\*distance product (GHz\*m), power consumption (mW/Gb/s/Port), and the technology comparison metric (Gb/s/mm<sup>2</sup>/port\*GHz\*m/mW/Port). Through simulations of electrical and optical link performance, which was verified through hardware testbeds, we have arrived at estimates for these metrics. We will show that optical interconnects offer a combined performance metric improvement greater than a factor of 25 over electrical interconnects.

## 2. ELECTRICAL AND OPTICAL LINK DECRPTIONS

### 2.1 Electrical link description

We developed electrical link [1], comprised of a transmitter (TX) and receiver (RX) chips, organic modules, pin via fields in the printed circuit board (PCB) under these modules and the transmission lines in the PCB (Figure 1). The transmitter and receiver are part of a 90 nm CMOS programmable chip with 16 channels in each direction and data rates up to 11 Gb/s. The transmitter has 3-tap feed-forward equalizer (FFE), while the receiver 5-tap decision-feedback equalizer (DFE). The link chips were mounted on organic modules, which were in turn mounted on PCB test vehicles with soldered BGA or land grid array (LGA) connections. We examined a wide variety of link topologies and lengths.

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The test vehicles were fabricated with a selection of advanced PCB materials (Megtron 6, Nelco 4000-13). The communication with the chips was through a digital link interface. This allowed optimization of the FFE coefficients, as well as data collection of link performance measures for later analysis.

We examined various link configurations, which included variable data rate, the amount of crosstalk, FFE and DFE equalization complexity, as well as modulation schemes (non-return to zero (NRZ) and duobinary). We conducted passive link measurements (link loss, crosstalk from dominant aggressors) on high speed PCBs manufactured with both Megtron 6 and Nelco 4000-13 materials and smooth copper (Figure 2).

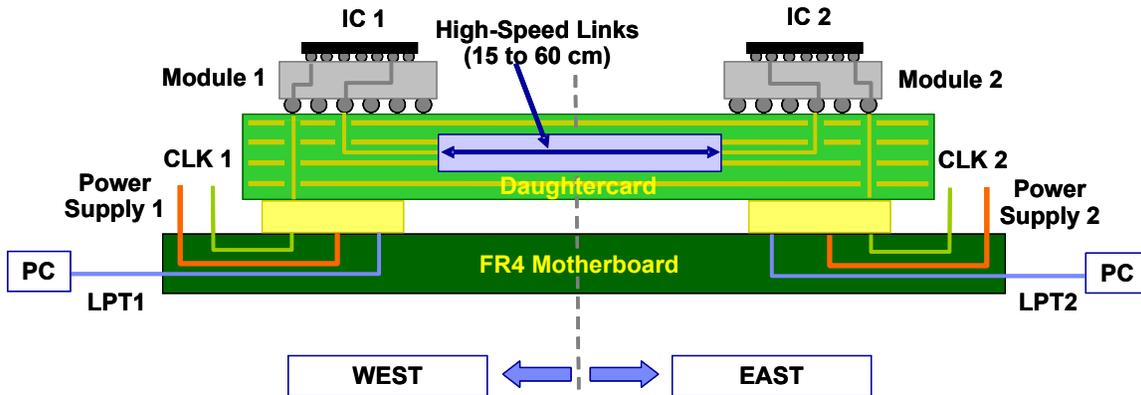


Figure 1. Experimental setup for the electrical link. Two modules, with 16 channels in each direction are connected on a high speed daughterboard. The distance between the channels is from 15 to 60 cm. All slow speed connections and control signals are on the motherboard.

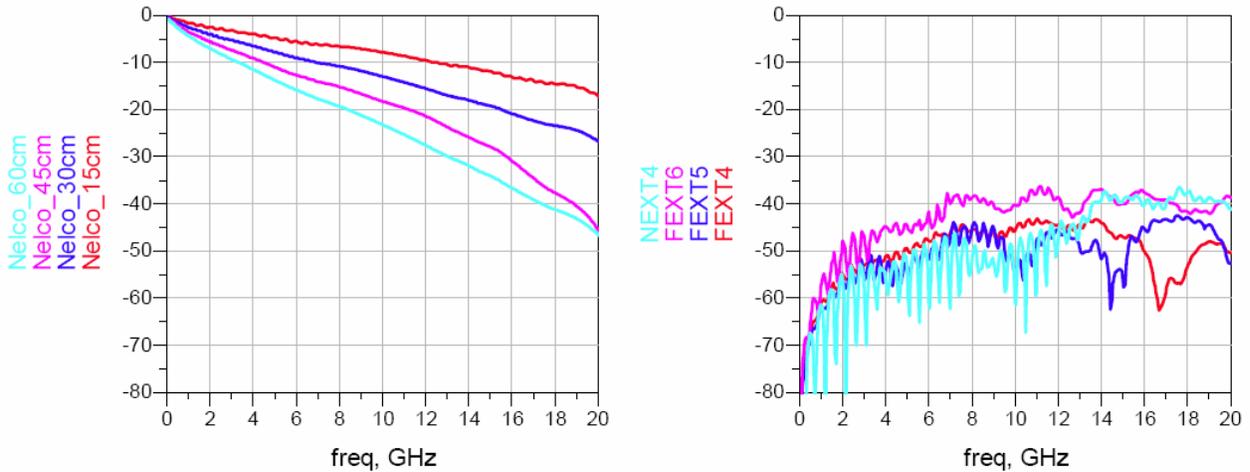


Figure 2. Channel response of a sample of module-to-module on-board electrical links. Link loss and crosstalk from several dominant aggressors are shown.

The electrical setup was used to correlate measurement and simulation results and verify our models. Representative sample of the results is shown on Figure 3. On the x-axis we show 8 electrical links, for two distances (45 and 60cm) and various levels of equalization complexity (no equalization, FFE only, DFE only and FFE+DFE). On the y-axis we show

the normalized vertical eye opening at a confidence level of  $10^{-3}$ . These comparisons show very good correlation, allowing us to extrapolate our results to longer links and other configurations for which we did not build hardware.

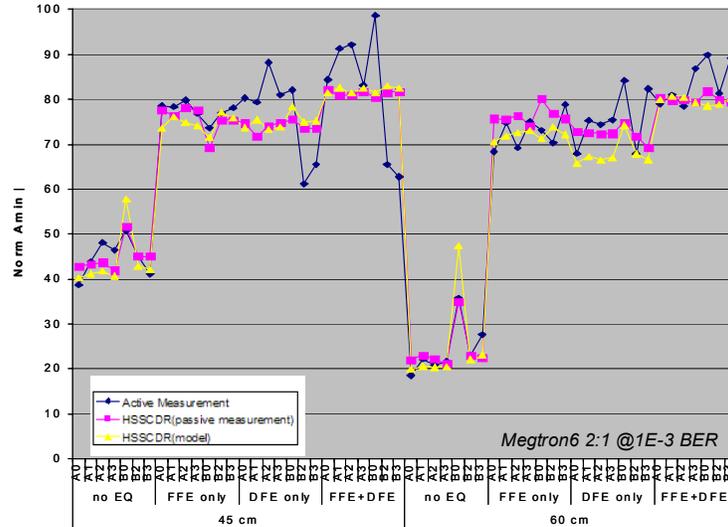


Figure 3. Comparison of hardware measurements and simulations in HSSCDR environment for various levels of signal processing in the transmitter/receiver. High degree of correlation was observed, allowing simulations of longer distances.

## 2.2 Optical link description

The experimental setup of the transceiver optical link [2] is shown in Fig. 4. The SLC transceiver package (Optomodule) includes the OE-IC assembly, or Optochip, that is flip-chip attached to the SLC carrier similar to conventional chip carriers. The Optomodule is a low-profile module directly surface mounted to a circuit board using a conventional ball grid array (BGA) solder process. The Optocard is formed of lens arrays and a dense array of optical waveguides with turning mirrors. Two Optomodules interconnected through the waveguides on the Optocard form a full link. The sixteen channel transceiver integrated circuit (IC) consists of independent laser-diode driver circuits and receiver amplifier circuits. Both the transmitter and receiver ICs are arrayed in separate 4x4 blocks with a 250- $\mu\text{m}$  x 350- $\mu\text{m}$  pitch, located at the center of the 5.25-mm x 3.25-mm IC. The periphery is reserved for bond pads on 200- $\mu\text{m}$  pitch. The 985-nm VCSEL and photodiode devices are also arranged on 4 x 4 arrays with the same 250- $\mu\text{m}$  x 350- $\mu\text{m}$  pitch.

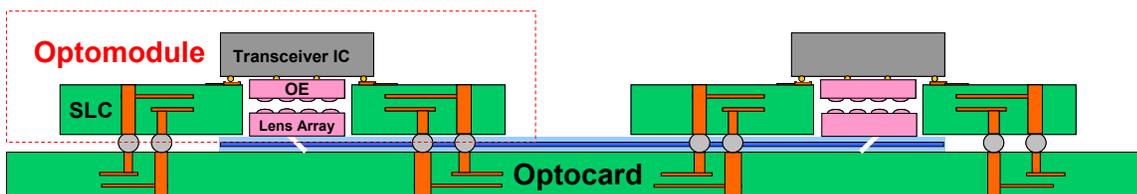


Figure 4. Experimental setup for the sixteen channel board-level optical link. The data is sent from the transmitter module, coupled into the waveguides by passing through the lenses and the turning mirrors, then back into the receiver module. The distance is between 30cm and 1m.

The polymer waveguides with  $35\ \mu\text{m} \times 35\ \mu\text{m}$  core dimensions were fabricated on the FR4 board with a pitch of  $62.5\ \mu\text{m}$ . The waveguide loss was less than  $0.05\ \text{dB/cm}$ . We also measured the bandwidth of the polymer waveguides by injecting short optical pulses generated by Ti:Sapphire mode-locked laser into single mode fiber and then into a  $2.55\text{m}$  long polymer waveguide [3]. The pulses were detected using a fast photodiode. The comparison of the input and output pulses is shown in Figure 5. From the time domain measurements we calculated the bandwidth of the polymer waveguide to be in excess of  $45\ \text{GHz}$ , allowing  $60\ \text{Gb/s}$  data transmission.

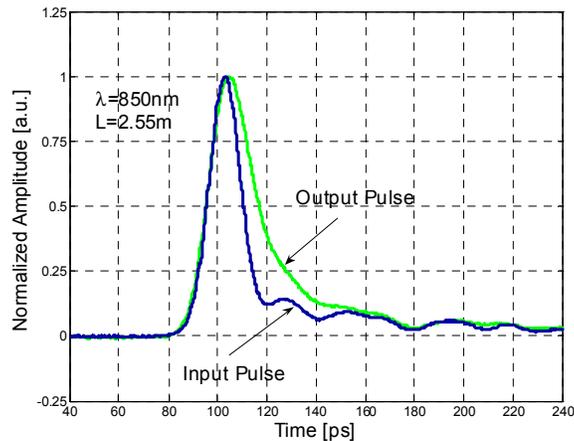


Figure 5. Measurement of the impulse response of a  $2.55\text{m}$  long polymer waveguide, whose bandwidth ( $>45\ \text{GHz}\cdot\text{m}$ ) was determined to be sufficient for  $60\ \text{Gb/s}$  transmission at  $1\text{m}$ .

The transmitter Optomodules were demonstrated to operate up to  $20\ \text{Gb/s}$ . The receiver was able to achieve speeds up to  $15\ \text{Gb/s}$ . We assembled full link and found that all 32 Optocard links were operating error free at  $10$  and  $15\ \text{Gb/s}$  with sufficient margin. At  $10\ \text{Gb/s}$  each link consumed  $13.5\ \text{mW/Gb/s}$ . The total power consumption was  $2.2\ \text{W}$ .

### 3. RESULTS AND METRICS COMPARISON

We first present results for the maximum achievable data rate for electrical and optical interconnects. Besides the implemented links and projections to higher data rates, we considered the ideal case for each (either no IC parasitics for the electrical, or the channel limit only for the optical interconnects) to gain insight into the possible space for improvements in the technology.

On Figure 6 we show the maximum achievable data rate for the electrical links, for two cases: the experiment hardware and the ideal case, with no IC parasitics. We considered distances up to  $120\text{cm}$  and when FFE and DFE are simultaneously used. In this case, above  $60\text{cm}$  the passive channel performance on the PCB limits the maximum achievable data rate, and there is very little incentive for improvement of the IC performance, since only marginal improvement is possible. However, below  $60\text{cm}$ , the picture is very different, and there is every reason to improve the performance of the ICs, that may lead to maximum achievable data rates above  $30\ \text{Gb/s}$ .

We generated similar curves for the optical interconnects (Figure 7). In this case, there is a wide gap between the performance of a link limited by the passive channel bandwidth (ideal case) and the optical link hardware. The EOE link is limited by the performance of the short electrical link, limiting performance to about  $26\ \text{Gb/s}$ . No FFE or DFE in this case were assumed on either end of the EOE link.

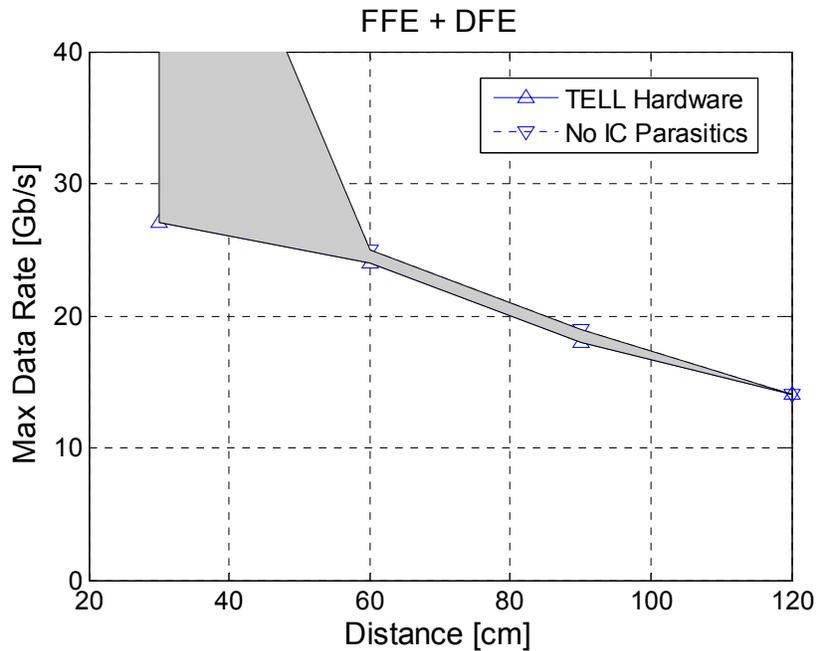


Figure 6. Maximum Data rate as a function of distance for electrical interconnects. The channel bandwidth limits the performance for distances above 60cm independent of IC hardware. Below 60cm improvements to IC hardware performance result in increased achievable data rate.

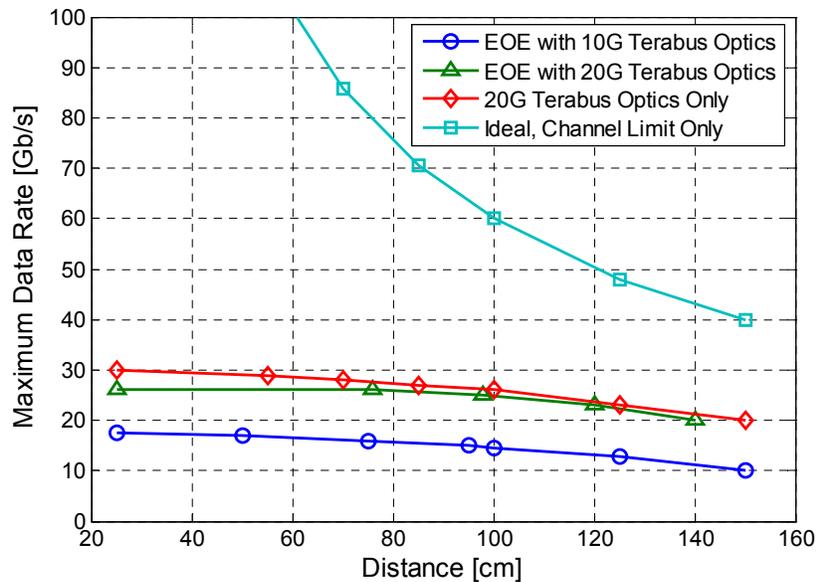


Figure 7. Maximum Data Rate as a function of distance for optical interconnects. Optical media is not the limiting factor in the link performance, leaving ample space for improvement of the rest of the components. Electrical link between the host and the optical modules limits the performance of the EOE link.

Measurements from the optical and electrical setups, as well as simulations, were used to verify some of the parameters we used in the metrics for comparison of optical and electrical interconnects for 100Gb/s class data transmission (Tables 1, 2). Only parallel NRZ solutions were examined. The first class of parameters for the metric comparison is related to area density. Here we examined the following parameters: a) silicon area devoted to I/O on module per port, b) silicon OE drive/receive circuit and OE area for the optics and electrical pad area for connection from organic package to circuit card for the electrical link, c) the total area on package, which is the sum of the previous two. In this group we can also put the bandwidth escape from the module (linear density). In both of these groups the optical interconnects have overwhelming advantage. The biggest advantage for the optical interconnects is the media distance\*bandwidth product, where the optics has almost an order of magnitude better metric. Another metric is the active link channel metric (in Gb/s\*m). This metric is comparable for both the electrical and optical interconnects for 10 Gb/s specified components, but the 20 Gb/s specified components give clear advantage to the optical interconnects.

The last entry is the technology comparison metric, which is the distance\*bandwidth/power, where the optics clearly wins.

Table 1. Comparison metrics for electrical and optical interconnects for 10 Gb/s specified components.

	Terabus (Optical)	TELL (Electrical)
Silicon area devoted to I/O on module per port (200µm pitch) [mm <sup>2</sup> /port]	< 0.48	0.24
Si OE drive/receive ckt & OE area [mm <sup>2</sup> /port]	0.175	0.00
Electrical pad area for connection from organic package to circuit card (1mm via pitch) [mm <sup>2</sup> /port]	0.00	3.00
Area on Package [mm <sup>2</sup> /port] (sum of above)	0.576	3.24
BW Escape from 50mm x 50mm module	38.4 Tb/s	5 Tb/s to 7.6 Tb/s (1mm LGA pitch)
BW Perimeter Escape Density (D) @ 10 Gb/s [Gb/s/mm] (note change from previous metrics)	192	25
Media distance*bandwidth/channel [GHz m] (single wavelength, no WDM)	>45	~ 12
Active Channel Gb/s*distance/channel [Gb/s-m] (limited by OE and I/O, no WDM)	>15	~ 14 (4-6 mill lines)
Power (80cm link) (P) [mW/Gb/s/Port]	< 3.7 + 7.5 = 11.2 Optical module + Processor = Total	12.5 (All in processor)
Technology Comparison Metric (D*BW/P) [Gb/s/mm peri * Gb/s-m / mW/Port]	192 * 15 / 75 = 38.4	25 * 14 / 125 = 2.8

Table 2. Comparison metrics for electrical and optical interconnects for 20 Gb/s specified components

	Terabus (Optical)	TELL (Electrical)
Silicon area devoted to I/O on module per port (200 $\mu$ m pitch) [mm <sup>2</sup> /port]	< 0.48	0.24
Si OE drive/receive ckt & OE area [mm <sup>2</sup> /port]	0.175	0.00
Electrical pad area for connection from organic package to circuit card (1mm via pitch) [mm <sup>2</sup> /port]	0.00	3.00
Area on Package [mm <sup>2</sup> /port] (sum of above)	0.576	3.24
BW Escape from 50mm x 50mm module	76.8 Tb/s	12 Tb/s to 15.2 Tb/s (1mm LGA pitch)
BW Perimeter Escape Density (D) @ 20 Gb/s [Gb/s/mm] (note change from previous metrics)	384	60
Media distance*bandwidth/channel [GHz m] (single wavelength, no WDM)	>45	~ 12
Active Channel Gb/s*distance/channel [Gb/s-m] (limited by OE and I/O, no WDM)	>26	~ 16.5 (4-6 mill lines)
Power (80cm link) (P) [mW/Gb/s/Port]	< (5 + 12.5) = 17.5 Optical module + Processor = Total	30.0 (All in processor)
Technology Comparison Metric (D*BW/P) [Gb/s/mm peri * Gb/s-m / mW/Port]	384 * 26 / 250 = > 40	60 * 16.5 / 600 = 1.65

#### 4. CONCLUSIONS

In this paper we compared the performance of electrical and optical interconnects for data rates in excess of 10 Gb/s/lane. We found that the technology comparison metric (distance \* bandwidth /power) is ~25 times better for the optical interconnects than for the electrical when 20 Gb/s specified optical components are used, and ~13.7 better when 10 Gb/s specified optical components are used. Most of the advantages for the optical over the electrical interconnects arise from the better bandwidth perimeter escape density and media bandwidth\*distance product for the optical interconnects.

#### 5. ACKNOWLEDGMENTS

The authors gratefully acknowledge DARPA support through contracts MDA972-03-3-0004 and HR0011-06-C-0074

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# Driver-receiver combined optical transceiver modules for bidirectional optical interconnection

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## ABSTRACT

We review a bidirectional optical link scheme for memory-interface applications. A driver-receiver combined optical transceiver (TRx) modules was demonstrated on an optical printed-circuit board (OPCB) platform. To select the bidirectional electric input/output signals, a driver-receiver combined TRx IC with a switching function was designed in 0.18- $\mu\text{m}$  CMOS technology. The TRx IC was integrated with VCSEL/PD chips for optical link in the TRx module. The optical TRx module was assembled on a fiber-embedded OPCB, employing a 90°-bent fiber connector for 90° deflection of light beams between the TRx module and the OPCB. The TRx module and the 90° connector were passively assembled on the OPCB, using ferrule-type guide pins/ holes. Employing these constituent components, the bidirectional optical link between a pair of TRx modules has been successfully demonstrated up to 1.25 Gb/s on the OPCB.

**Keywords:** Optical transceiver, bidirectional optical link, driver, receiver, transceiver module, optical PCB

## 1. INTRODUCTION

PCB-compatible optical interconnection has been studied for chip-to-chip and board-to-board optical link in high speed and large capacity data-processing systems.<sup>1-4</sup> In the electrical interconnection between LSI chips (*e.g.* memory and microprocessor chips) through a large number of electrodes, the input and output signals are bidirectionally transmitted in time division through one input/output (I/O) line. However, in the optical interconnection the bidirectional transmission through one optical line could be inefficient since it requires bulky optics for coupling and splitting of input/output lights. Thus, a bidirectional optical transmission through separated input and output lines could be a reasonable solution. For this optical transmission scheme we need bidirectional transmitter/receiver ICs with a switch function for input/output electrical signals. However, the previous works<sup>5-7</sup> have employed separated unidirectional chips such as a pair of Tx and Rx ICs. These Tx/Rx ICs does not have the switching function to deal the bidirectional electrical signals for real memory or microprocessor chips. Furthermore, the separate Tx/Rx ICs occupy a large packaging area to link the bidirectional electrical signals to the separated optical lines. To alleviate these problems, we have designed to integrate the Tx and Rx circuits on a single chip by employing a selection switch (SW) and using a proposed common gain stage<sup>8</sup>. The driver-receiver combined transceiver (TRx) IC was fabricated using Si-CMOS transistors. This bidirectional TRx IC could also reduce the overall power dissipation as well as the chip area, compared to the separated Tx/Rx ICs.

In the PCB-based optical interconnection systems, most of the works have been studied on-board connection types in which the optical layers are exposed to the surface of the PCBs.<sup>1,4</sup> These on-board interconnection schemes could limit the area and space for surface mounting of other chips on the PCBs. For more compact integration, we demonstrated optical-layer-embedded boards<sup>9-14</sup> where silica-fibers are laminated in conventional FR4 electrical boards. To couple lights between the optical boards and surface-mounting optical transceiver/receiver (Tx/Rx) modules, a 90°-bent fiber block was proposed,<sup>9-12</sup> which is assembled in the fiber-embedded board. A packaging solution was also proposed to achieve passive assembling of the connectors and Tx/Rx modules in/on the optical PCB (OPCB).<sup>11</sup> The connectors and modules were coupled utilizing the guide pins/holes of conventional mechanically-transferable (MT) ferrules being used for fiber ribbon connection. This passive assembling scheme was applied to demonstrate the bidirectional optical link using the driver-receiver combined TRx modules on the optical PCB. We review the design issues and packaging strategy for the bidirectional optical link.

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## 2. BIDIRECTIONAL OPTICAL LINK SCHEME

Figure 1 shows the bidirectional optical link scheme based on the OPCB. The proposed scheme consists of optical TRx modules, optical connectors, and an OPCB. The signal flow of the optical link from TRx1 module to TRx 2 module is given by a series of steps in the following order: (1) TRx 1 module with a VCSEL array and a TRx 1 IC chip; (2) optical connector; (3) embedded optical layer; (4) optical connector; and (5) TRx 2 module with a PD array and a TRx 2 IC chip. Signal flow to the reverse direction can be also given from TRx 2 module to TRx 1 module. The input/output electrical signals transferred through a bidirectional electrical line are converted to/from optical signals in the TRx modules and they are separated into the optical input and output lines, as seen in Fig. 1(b), by the switching function of the TRx ICs.

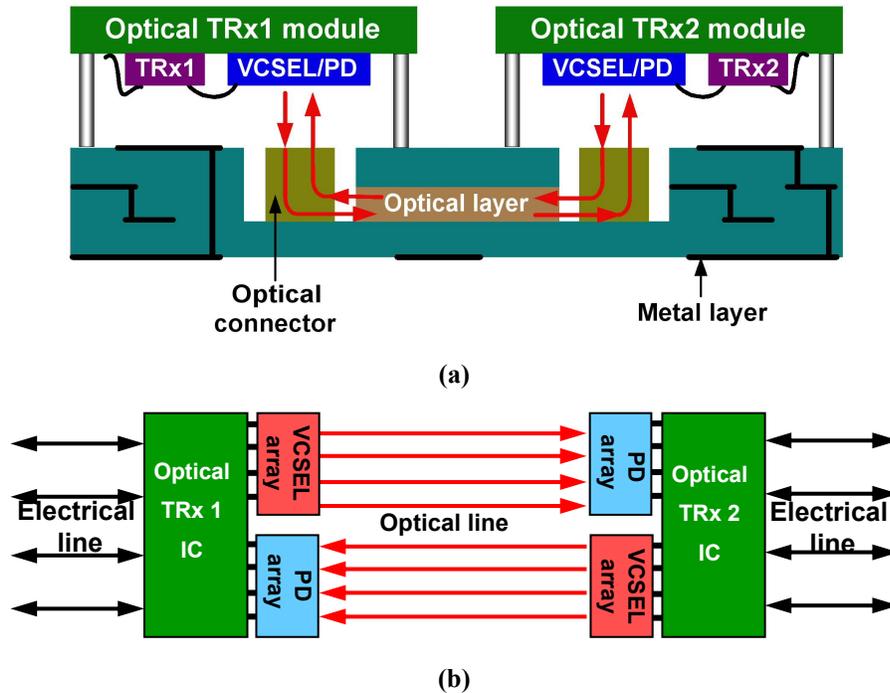


Fig. 1. (a) Side view and (b) top view of the bidirectional optical link scheme on the OPCB.

## 3. DESIGN OF DRIVER-RECEIVER COMBINED TRANSCEIVER IC

Figure 2 shows the block diagram of the driver-receiver combined TRx IC we proposed. A typical limiting amplifier on the Rx part, for amplifying and reshaping the output signal of a trans-impedance amplifier (TIA), consists of an input stage, a limiting stage, and an output stage. On the Tx part, the typical structure of the driver is similar to that of the limiting amplifier, except that the output stage directly drives the VCSEL with sufficient bias and modulation currents. Hence we have designed a driver-receiver combined optical transceiver IC to share the common block, *i.e.* gain stage, between the limiting amplifier and the driver.<sup>8</sup> It is a feasible design strategy since the optical input for the Rx mode and the electrical input for the Tx mode are multiplexed in time division for the chip-to-chip optical link. Furthermore, a crosstalk problem between a Tx and a Rx concurrently operating in a single chip is not serious in this transmission system. As shown in Fig. 2, the proposed CMOS TRx architecture consists of input stages for an electrical signal and an optical signal, a common gain stage, and output stages with the selection control switch. The TRx interfaces with external components, such as the PD and TIA on the Rx side, and the VCSEL on the Tx side.

The common gain stage must be capable of sufficiently amplifying small amplitude signal with adequate gain for the Rx mode and providing limited signal amplitude to drive the VCSEL for the Tx mode. In order to meet these requirements,

the common gain stage is designed to offer sufficient gain and bandwidth for the input signal, and the output stage is designed to interface the circuit with the subsequent input stage. The common gain stage has three stages in this work. Both the first and third stages are adopted to achieve high gain and wider bandwidth using a Cherry-Hooper topology modified with an inner cascode amplifier. The inner cascode stage is a cascade of a common-source amplifier and a common-gate amplifier, which offers the higher bandwidth by minimizing the Miller capacitance. For the second stage, a common-source differential amplifier is used to provide higher gain.

The output stage consists of the electrical buffer and the optical output driver. The electrical buffer acting as a source follower provides an impedance matching with a subsequent circuit. The optical output driver consists of an open-source driver to modulate the VCSEL current, a current source to deliver a prebias current to the VCSEL, and a source follower with a resistive load corresponding to a dummy driver. One of both outputs is selected by the SW depending on the operating mode. A careful design is required for isolation between the enabled and the disabled ports, since the disabled input may affect the output through the shared circuit block. The disabled signal, if any, feeding to the TRx circuit could be regarded as a noise, of which the effect could be minimized by using a differential pair in the circuit. While the electrical output buffer uses a 1.8 V supply, the optical output driver operates at a supply voltage of 3.3 V to accommodate comparatively high forward voltage of the VCSEL.

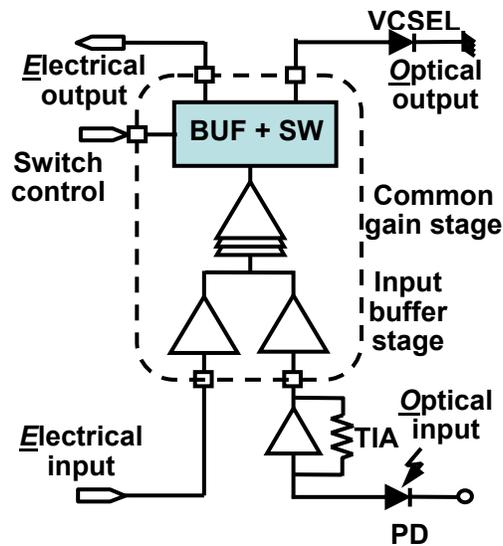


Fig. 2. Block diagram of a driver-receiver combined TRx IC.

The TRx IC was fabricated using a commercial 0.18- $\mu\text{m}$  Si-CMOS technology. Fig. 3 shows a photograph of whole chip of the TRx. The occupied chip area is 0.82 x 0.82 mm<sup>2</sup>. The design strategy that shares the common block of the limiting amplifier and the driver contributes to a chip-area reduction of over 30% and makes it possible to save 55% or 20% of power dissipation, depending on the Tx and Rx mode compared to the unshared transceiver.<sup>8</sup>

The TRx was first tested on-chip using GGB microwave probes in order to verify the performance of the chip itself. The external devices including the VCSEL and the PD/TIA are connected with high-performance RF cables. The frequency responses for two operating modes of the TRx chip are illustrated in Fig. 4. The -3-dB bandwidths of the Tx and Rx modes are, respectively, 2.2 GHz and 2.4 GHz. From the small signal measurement, the disabled outputs for the Tx and Rx modes were isolated with -25 dB and -48 dB at -3-dB bandwidth, respectively, from the enabled output.

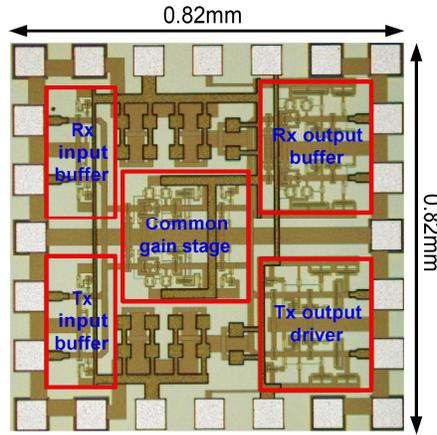


Fig. 3. A photograph of the fabricated CMOS TRx IC.

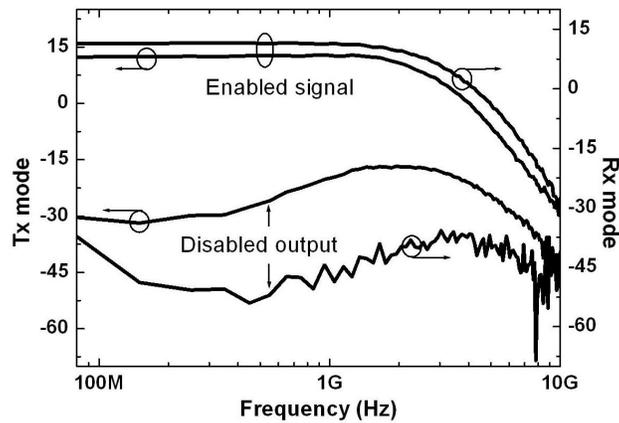


Fig. 4. Small-signal frequency response gain of the enabled and disabled outputs for respective Tx and Rx modes.

#### 4. BIDIRECTIONAL TRANSCEIVER MODULE

Figure 5(a) shows the packaging structure of the bidirectional TRx module which is assembled on the optical connector and the OPCB. For passive assembling of the module and the connector on/in the OPCB parts, MT ferrules with guide pins/holes were employed for accurate alignment of each component, as described in the previous work.<sup>11</sup> The VCSEL and PD chips on the module were positioned between guide holes on the module side, matching to the center positions of the fibers which will be located between the guide holes on the connector side.

Figure 5(b) shows an inside picture of the TRx module where the TRx IC was integrated with 1 x 4 arrays of 850 nm VCSELs and PIN PDs. Since our prototype TRx IC was designed for a single channel of optical input and output, the IC was contacted to a pair of VCSEL/PD devices among the 1 x 4 array devices. For the bidirectional link, the VCSEL and PD array chips are linearly integrated between the guide holes. The VCSEL and the PD array chips were precisely die-bonded on the metal layer so as to align them above the optical connector. The metal layer contributes to a heat sink and common ground node for the VCSEL. The spacers on the both side of the VCSEL and PD chips were attached to prevent the bonding wires from being damaged on assembling the TRx module and the OPCB. The module-to-OPCB electrical connection was achieved with hollow metal pins which are located on outsides of the spacer.

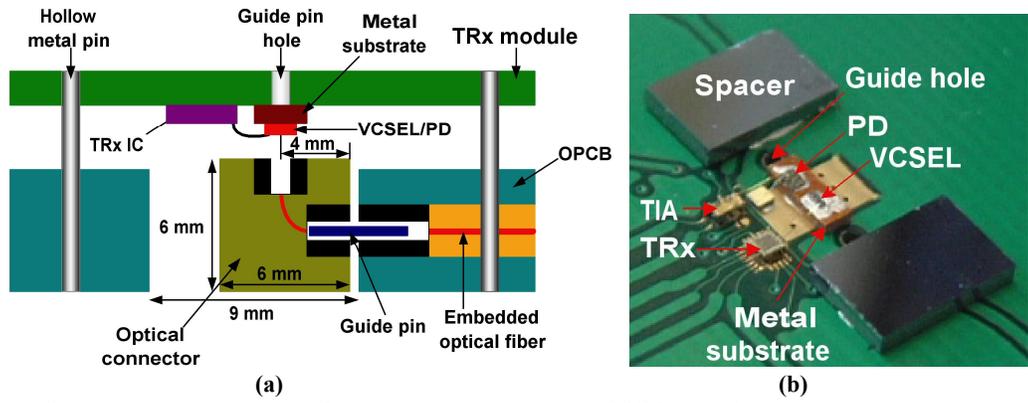


Fig.5. (a) Schematic structure of the TRx module assembled on the OPCB and (b) a photograph of chips integrated in the TRx module.

### 5. OPTICAL PCB AND CONNECTORS

To provide bidirectional optical paths in the main board, we fabricated a 1-layer fiber-embedded PCB. The fabrication process shown in Fig. 6 is follow: (1) construct a 7.5-cm-long fiber array terminated by MT ferrules with 1 x 12channels an a channel pitch of 250- $\mu\text{m}$ ; (2) cut a groove to place the fiber array and ferrule on a bottom FR4 PCB; (3) cap a top FR4 PCB; (4) laminate using the conditions of multilayer PCB processes, which are pressed at the pressure less than 47 kg/cm<sup>2</sup>, at the peak temperature of 180°C, for 1 hour; and (5) form square through-holes to expose the cross-section of the ferrule in the OPCB.<sup>12</sup> Figure 7 shows the Ferrule and fibers exposed to the side wall of the square through holes. The used fiber was a commercialized 1 x 12 multi-mode silica fiber array with a core/clad diameter of 100/110  $\mu\text{m}$  and 7.5- $\mu\text{m}$  thick polyimide coating layer.<sup>12-14</sup> The OPCB used in this work consists of four electrical layers for signal and power/ground, and one optical layer.<sup>11,12</sup>

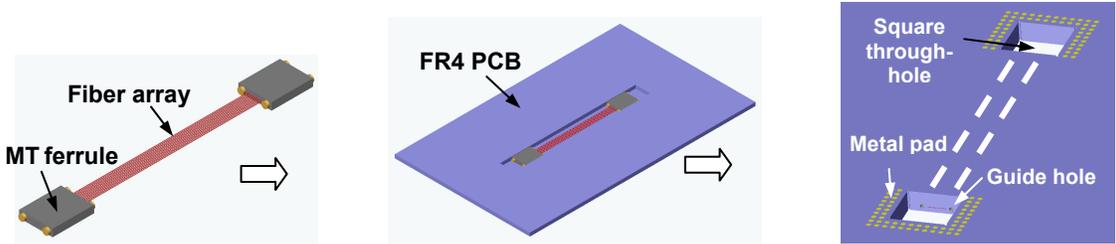


Fig. 6. Fabrication process of the fiber- and ferrule-embedded PCB.

The 90°-bent fiber connector was fabricated using the same fiber array with that used in the OPCB. Fig. 8 shows a photograph of the 1 x 12 90°-bent fiber connector used in our platform. The multimode fibers mounted with two MT ferrules was bent and inserted into an aluminum block. The guide pin of the MT ferrule mounting the fibers guarantees an accurate alignment of optical paths within  $\pm 1 \mu\text{m}$  when the connector is assembled between the TRx module and the

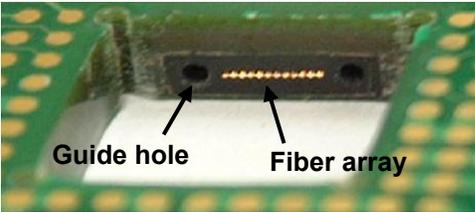


Fig. 7. Photograph of the fiber- and ferrule-embedded PCB.

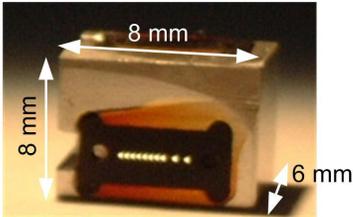


Fig. 8. Photograph of the 90°-bent fiber block.

OPCB. The radius of the curvature of the bent fibers was about 3.5 mm and the bending loss was about 0.1 dB. The size of the block was  $6 \times 8 \times 6 \text{ mm}^3$ . The insertion loss of the connector was measured less than 0.5 dB, including the fiber bending loss and scattering losses at the interfaces between the module and the connector and between the connector and the OPCB. This insertion loss is sufficiently low for optical interconnection purposes. In this connector, 1 x 12 linear array of fibers is mounted. Among these 12 channels, a pair of channels was used for bidirectional optical paths coupled to the VCSEL and PD in the TRx module.

## 6. BIDIRECTIONAL OPTICAL LINK PLATFORM

The function of the bidirectional optical link for the bidirectional TRx ICs were test using a pair of the TRx modules, TRx 1 and TRx 2, which are configured as Fig. 9. The bidirectional optical link platform constructed on the OPCB is shown in Fig. 10. Transmission of the bidirectional input/output signals were examined through a couple of differential lines. The coupled differential lines are denoted by bars on the number. The TRx modules were assembled flipping on the OPCB as shown in Fig. 10. All Tx inputs and Rx outputs are attached with SMA connectors to interface with measurement equipments such as pulse pattern generator and oscilloscope.

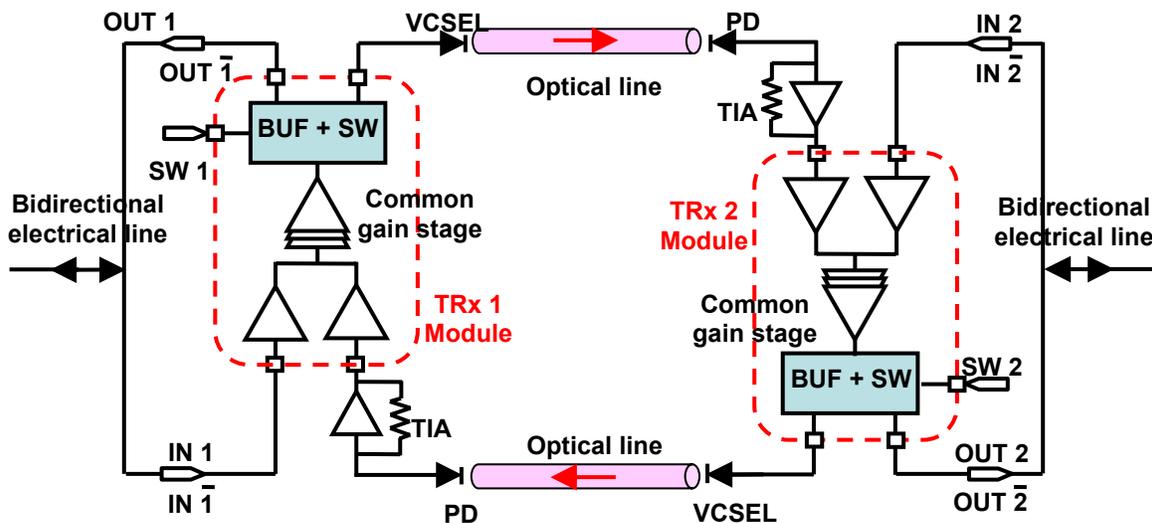


Fig. 9. Configuration of electrical lines, optical lines, and TRx modules constructed in the bidirectional optical link platform.

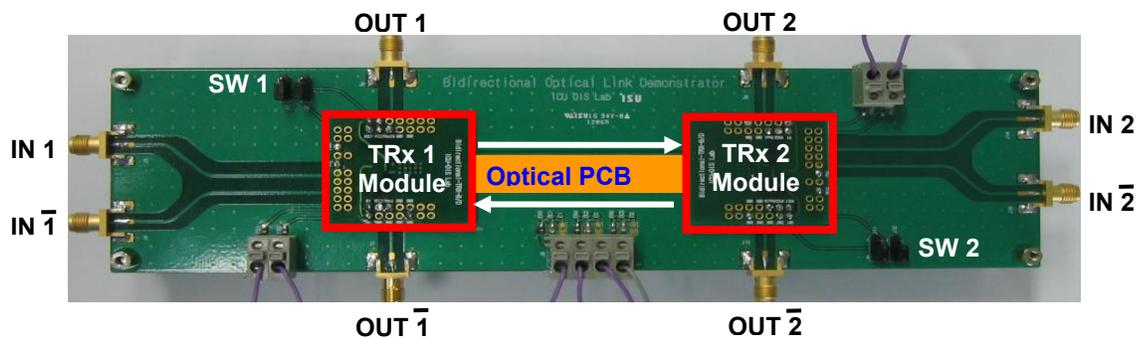


Fig. 10. Bidirectional optical link platform constructed with a pair of the bidirectional TRx modules on OPCB.

Figs. 11(a) and (b) show the measured 1.25 Gb/s eye diagrams for TRx 1-to-TRx 2 and TRx 2-to-TRx 1 transmissions, respectively. The output amplitude is about 320 mV<sub>pp</sub>. Peak-to-peak jitters of both transmissions are 280 ps and 275 ps, respectively. The BER performance achieved less than 10<sup>-12</sup> at bidirectional transmission of 1.25 Gb/s data rate.<sup>12</sup>

These results show successful bidirectional transmission through TRx IC and optical PCB system of our interconnection scheme. However, the eye diagrams showed a lower performance compared to the simulated performance of the driver-receiver combined TRx. The reasons could be as follows: (1) parasitic inductances due to long bonding wires between the bidirectional TRx and the optical devices; (2) an impedance discontinuity due to AC-coupling capacitors between the transimpedance amplifier and the bidirectional TRx; and (3) the bandwidth limit of the electrical signal path, including signal line on FR4 PCB and the metal hollow pin. Hence, improvements in design regarding these problems could lead a better performance in bidirectional transmission on the optical PCB system.

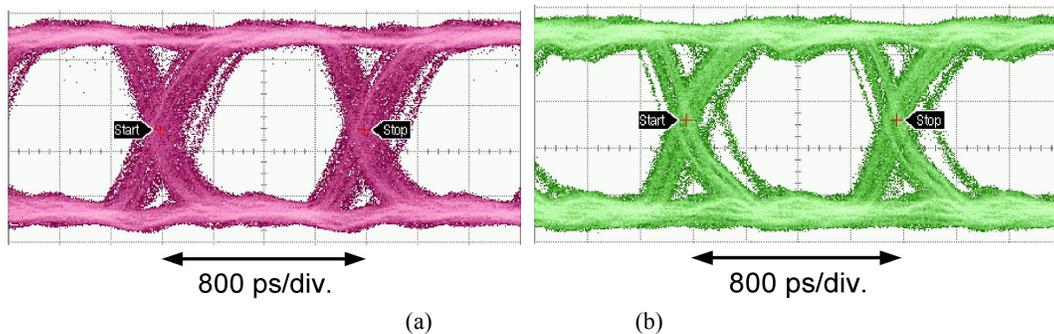


Fig. 11. Measured eye diagrams for bidirectional optical link of 1.25 Gb/s signals through OPCB: (a) TRx 1-to-TRx 2 and (b) TRx 2-to-TRx 1 transmissions.

## 7. CONCLUSION

A bidirectional optical link structure based on the optical PCB has been proposed for application to chip-to-chip interconnections. For the bidirectional optical link, various components were devised: a driver-receiver combined TRx IC, a VCSEL/PD integrated TRx module, a 90°-bent fiber connector, and fiber-embedded optical PCB. The guide pin/hole structure were employed for passive assembling of the TRx module, the 90°-bent connector on the OPCB. Using this assembling scheme, we achieved an accurate alignment and a low connection loss for the bidirectional optical paths. Bidirectional link performance up to 1.25 Gb/s operation between a pair of the TRx modules has been demonstrated. Improving signal integrity on the electrical signal path could lead to higher link performances. The proposed bidirectional optical-link structure on the PCB opens up an opportunity for high-speed optical-link computer system. Also, the fusion of the fiber-optic technology with the PCB technology could open the realization of cost-effective and high performance optical interconnection systems.

## ACKNOWLEDGMENTS

This work was supported by the National Program for Tera Level Nano Devices and partially by Korea Research Foundation Grant (KRF-2004-042-D00258).

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