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## LONG LINEAR MWIR AND LWIR HgCdTe INFRARED DETECTION ARRAYS FOR HIGH RESOLUTION IMAGING

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**RESUME** - Cette publication présente les derniers résultats obtenus au LETI / LIR (laboratoire Infrarouge) sur le développement de grandes barrettes linéaire destinées à des applications d'imagerie Infrarouge à haute résolution. Les prototypes réalisés possèdent 1500 détecteurs (longueur  $\approx$  50 mm) opérant dans les bandes spectrales 3-5 and 8-10  $\mu$ m; ils présentent une architecture hybride indirecte comportant des circuits de détection HgCdTe PV et des circuits de lecture Si CMOS hybridés sur un réseau d'interconnexion. L'aboutage précis des différents circuits, avec respect du pas des détecteurs, est effectué au moyen de techniques performantes de découpe rapprochée et d'interconnexion, spécialement développées pour cette application

**ABSTRACT** - High resolution infrared imaging system calls for very long scanning arrays with several thousands of detectors and high performance. This paper presents the recent technological developments and the electrooptical performances obtained at LETI / LIR (Infrared Laboratory) on 1500 detector linear HgCdTe arrays working in the 3-5 and 8-10  $\mu$ m spectral ranges. These very large arrays (length  $\approx$  50 mm) have an indirect hybrid architecture composed of butted HgCdTe PV detection circuits and Si CMOS readouts hybridized on a fanout substrate. Defect free dicing and butting, respecting the detector pitch, is made by accurate and non damaging techniques.

### 1. INTRODUCTION

The high performance and current technical maturity of HgCdTe/CMOS infrared detectors are such as to envisage the manufacturing of large format sensors dedicated to high-resolution IR imaging for space applications.

Earth observation from satellites for both civil and military missions in the area of earth environmental monitoring, resource surveys, meteorology or surveillance calls for high spatial and radiometric resolution. The sensors adapted to these applications are long linear arrays with several thousand detectors, generally used in scanning mode of the pushbroom type

### 2. IR DETECTORS DEVELOPMENT AND MANUFACTURING IN FRANCE

SOFRADIR, the specialist in development and manufacturing of Infrared Focal Plane Arrays based on HgCdTe material, uses in production a technology which was developed and is still under improvement at LIR

The French activity in the field of military tactical applications is worldwide well known contrary to space applications. Nevertheless LIR and SOFRADIR are involved in different space programs supported by the French Ministry of Defence (DGA), the CNES, the European Space Agency (ESA) or industrial companies

Three types of application can be considered:

- application for which "off the shelf" components can be used. It was recently the case of the Cimex (Bresilian space agency) and Clementine 2 (Cedip/LLNL/NASA - USA) programs,
- application for which a specific development is necessary on the basis of proven technologies. It is the case of the Helios 2 program (DGA France),
- application for which a specific development is necessary on the basis of very advanced concepts and technologies. It is the case of several study phases of programs in progress

Due to this situation, SOFRADIR is in position to propose a large possibility of answers to potential customers from the "poor" scientist people to the "very demanding" programs.

Concerning long butted IR arrays, the LIR is involved in a program of technological development and feasibility study. The first butted demonstrators with several hundred pixels have been fabricated in the 11.5 to 12.5  $\mu\text{m}$  spectral range within the frame of studies carried out for the CNES [Cham 92] and for the ESA - ESTEC [Dava 95] (HRTIR project). In parallel with these studies, work is currently in progress on the development of two butted detection arrays with 1500 pixels operating in the spectral range 3-5 and 8-10  $\mu\text{m}$  for use in an airborne measuring instrument developed by ONERA [Cham 97].

### 3. ARCHITECTURE OF LONG BUTTED LINEAR ARRAYS

The requirements for imaging call for linear arrays with several thousand pixels offering very high performance, high operating characteristics (few or no defects) and perfect reliability.

The current unavailability of very large dimension HgCdTe detection circuits or Si readout circuits makes it impossible to manufacture large focal plane arrays as monolithic units. In addition, such a HgCdTe / Si monolithic structure, 5 centimeters long or more, would be subject to high thermomechanical stress resulting in uncertain reliability.

In contrast, a modular butted structure is perfectly adapted to large dimensions and is very versatile. This modular approach can in fact be retained for a large variety of components of various complexities, operating in various usual IR spectral ranges (2 to 15  $\mu\text{m}$ ).

The modular focal plane developed at LETI / LIR has an indirect hybrid structure made up of three sub-assemblies (figure 1):

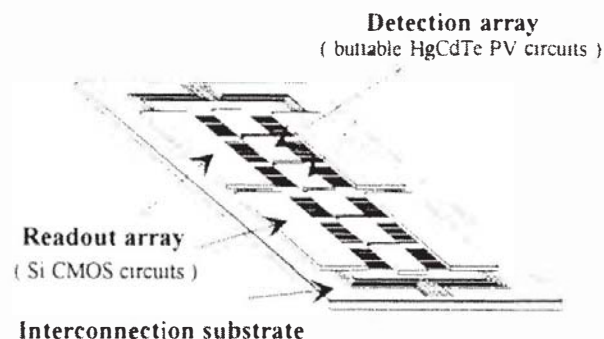


Figure 1 hybrid focal plane of long linear IRCMOS detection array

- An IR detection linear array consisting of several HgCdTe detection circuits aligned and butted together. The aim is to realize a perfectly continuous detection line which respects the arrangement of the detectors. In particular, in the butting zone the detector pitch must be conserved without any pixel loss. This latter condition is, of course, a major technological difficulty which can only be achieved using very high-performance butting techniques.
- A signal processing array consisting of silicon readout circuits juxtaposed along the detection zone. Perfect butting is not essential and several simple solutions can be adopted to enable the circuits to be spaced out enough. This can be achieved by reducing the pixel pitch compared to the readout pitch or even by modifying the spread of the readout connections on the interconnection substrate.
- An interconnection substrate which takes care of the mechanical support and the electrical interconnection of the various circuits. These two functions are performed by indium bumps and metallic tracks which link each detector to an input stage of the readout circuits. The choice of an appropriate material for this substrate enables the mechanical reliability of the component to be optimised by reducing the impact of the differential thermal expansion induced by the HgCdTe and Si circuits.

#### 4. BUTTING TECHNOLOGIES

The manufacturing of these focal plane arrays requires the use of techniques of butting which have been specially developed for HgCdTe detectors.

In fact, the greatest technological difficulty concerns the process of butting of the different HgCdTe detection circuits while respecting the overall detector pitch without creating defects. Meeting this objective requires mastering both the dicing process of the elementary HgCdTe modules and their positioning and interconnection on the support. These operations must be carried out with a quasi-micronic precision and must not degrade the performance of the detectors.

Dicing the HgCdTe circuits within a few microns of the edge pixels (at around 25  $\mu\text{m}$ ) is a delicate operation which cannot be carried out with conventional commercial techniques (sawing, lapping). This difficulty is related to the high sensitivity of the HgCdTe material to mechanical perturbations which generate crystalline defects causing a degradation of the electrical properties of the detectors (leakage current). This sensitivity to perturbation obviously increases when the material bandgap shortens; this makes the dicing operation particularly critical for the 8 - 10  $\mu\text{m}$  detectors. A specific dicing technique has been developed at LIR and enables the electrical performance of the detectors to be conserved while offering a dicing precision of the order of 2  $\mu\text{m}$  (StdDev).

The assembly of the different circuits on the interconnection stage is carried out by hybridization using indium bumps. This technique which provides an interconnection success rate of 100% is now widely used in the manufacture of infrared components. Substantial improvements have been implemented to enable collective hybridization of the circuits with very high precision [Tiss 96]. In particular, a self-alignment procedure operates during the hybridization [Mari 94] which helps to correct any misalignment due to the presentation of the different circuits. The final positioning precision of all the detectors, with respect to their theoretical positions is better than 1  $\mu\text{m}$  (in the X,Y plane of the interconnection stage). In the orthogonal axis, the elevation Z of the detectors is controlled by the height of the indium bumps with a precision of about 2  $\mu\text{m}$  (StdDev).

#### 5. PROTOTYPES OF LONG HgCdTe BUTTED LINEAR ARRAYS

Two butted IRCMOS linear arrays with 1500 pixels working in the 3-5 and 8-10  $\mu\text{m}$  spectral ranges have recently been made at LIR with the aims of validating the concept of the modular FPA,

implementing the butting technologies and evaluating the performance of this type of detection array. These prototypes have a *large detection zone of 45 mm in length*, and are composed of 5 and 10 butted HgCdTe circuits (respectively for the 3-5 and 8-10 array) and 5 CMOS readout circuits, hybridized onto a sapphire interconnection substrate

The alignment precision of all the pixels compared to their theoretical position is of the order of 1  $\mu\text{m}$ . The pitch of the detectors is maintained along the whole length of the linear array respecting the staggered topology [Cham 97].

The main characteristics are given hereafter and a general photograph of the 3-5  $\mu\text{m}$  butted array is shown in figure 2

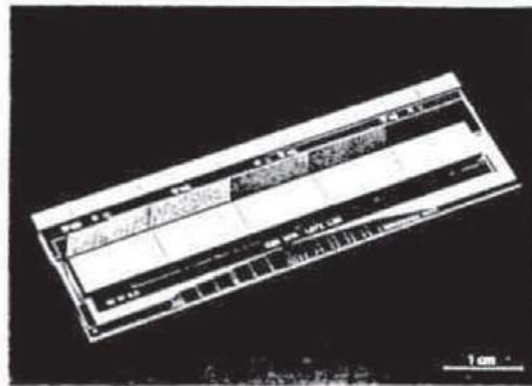


Figure 2 1500 element linear MWIR HgCdTe/CMOS array

### 5.1. HgCdTe detection circuits

The detection material is an epitaxial layer of HgCdTe made using a liquid phase growth technique on a CdZnTe lattice-matched substrate. This growth procedure used in LIR and SOFRADIR enables material to be produced with high electrical and crystalline qualities

The detectors are photovoltaic N/P homojunctions made by ion implantation on the P-type HgCdTe material. The detectors have an active surface of  $30 \times 30 \mu\text{m}^2$  and are laid out in a staggered arrangement with a linear pitch of 30  $\mu\text{m}$ .

### 5.2. Si readout circuits

Each CMOS readout circuit of the butted components multiplexes 300 detectors. The input stages take care of coupling with the detector, integrating its current and transforming the resulting charge into a voltage. The output voltages of these stages are multiplexed to a single output stage.

The coupling of the detector is carried out by direct injection. Several charge to voltage conversion ranges carried out by a set of integrating capacitors selectable by switches are used in order to respond to a large spread of operational conditions.

A switch implanted between the integration capacitors and a switched follower are used to sample and hold the signal at the end of the integration time on the capacitor. Thus, it is possible to begin a new integration cycle while the samples of the previous one are multiplexed towards the output stage.



The output voltages from each input stage are successively read through a PMOS source follower selected by the binary address decoder and fed to the output amplifier. The output amplifier is realized from an operational amplifier with a unity gain feedback.

A specific adaptative biasing function have been implemented in this circuit. The aim of this biasing technique is to correct a few defective detectors which may exist in the LWIR spectral range. Among these detectors, some exhibit leakage current excess which leads to a "blind" pixel due to the saturation of the storage gate (although they can detect), some others exhibit extra 1/f noise which leads to decrease the signal to noise ratio.

The adaptative biasing allows to bias separately each detector and makes it possible to optimize each detector operating point with respect to the noise or to avoid saturation. The bias voltage can be sampled and held on the coupling transistor gate. Two bias direct injection modes are possible. The first one is the standard mode where the detectors are biased all together at the same voltage. The second mode allows to fit separately each polarisation detector by using the address binary decoder to validate the correct input stage.

The experiment results demonstrate the very good repeatability of the bias function between several uses.

The circuit was processed in a 1.2  $\mu\text{m}$  CMOS technology (Thomson-TCS France). This is a one-poly two-metal layer technology with a maximum supply voltage of 5 volts with analog capacitors (polysilicon-over-diffusion capacitor type).

The pitch of the input stages is 27  $\mu\text{m}$ , whereas the pitch of the detectors is 30  $\mu\text{m}$ , in order to avoid precise butting of the readout circuits.

### 5.3. Interconnection substrate

The interconnection substrate is a passive circuit realized on sapphire wafers in the microelectronics foundry of LIR. Sapphire was chosen for its thermomechanical properties and its adaptability to HgCdTe and Si circuits of similar dimensions.

The circuit has a simplified topological structure comprising two metal levels (HgCdTe detector-Si readout metal lines and indium bump connections). No major technological difficulty is encountered in the manufacture, but special attention must be paid to number of defects. This is quite a critical point given the large size of the circuit (50 x 15 mm<sup>2</sup>). Zero defect circuits are selected using an automatic point test for continuity and insulation, which determines the integrity of the 1500 detector-readout connections and the control lines of the circuits.

## 6. PERFORMANCE OF THE 1500 ELEMENT MWIR IRCMOS BUTTED ARRAY

In this section we present the electrooptical results obtained on the 1500 detector butted linear arrays operating in the 3-5  $\mu\text{m}$  waveband.

All the characterisations were carried out with an extended test pattern at 293 K and 300 K. A 16-bit 100 kHz digitiser was used to obtain acquisitions at pixel frequency with a 100  $\mu\text{V}$  LSB. The measurement of rms noise was made in the 0.5 Hz to 200 Hz range, the high value 200 Hz being the image frequency of the component. The measuring conditions as well as the main characteristics of the component are given in the following table.

operating temperature	78 K
field of view	28°
cutoff wavelength	5.5 $\mu\text{m}$
frame frequency	200 Hz
pixel frequency	62.5 kHz
integration time	5 ms
charge handling capacity	7.3 $10^7$ e <sup>-</sup>

Figure 3 and 4 give the histogram and the NEDT cartography respectively measured at half range i.e. for a charge stored in the pixel of  $3.7 \cdot 10^7$  electrons. This parameter is obtained for each detector by the direct ratio between the rms noise and the output response.

The mean value of 4.3 mK obtained is very close to the theoretical value corresponding to the charge stored in the pixel, the degradation being less than 10%. One can see on the NEDT cartography the very small number of defects: 3 outright defects, i.e. 99.8% operability and only 6 detectors with an NEDT greater than 10 mK. In particular, no circuit-edge defects were created by the butting procedure.

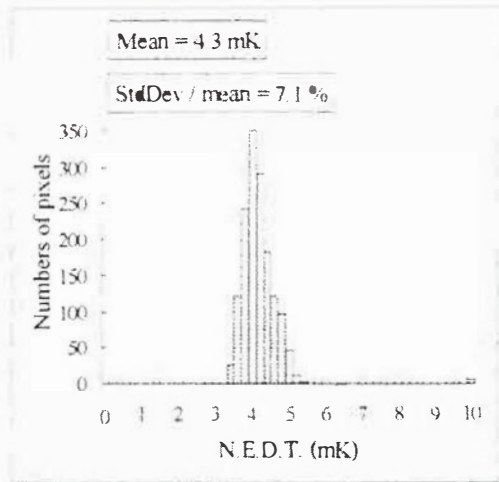


Figure 3: NEDT histogram

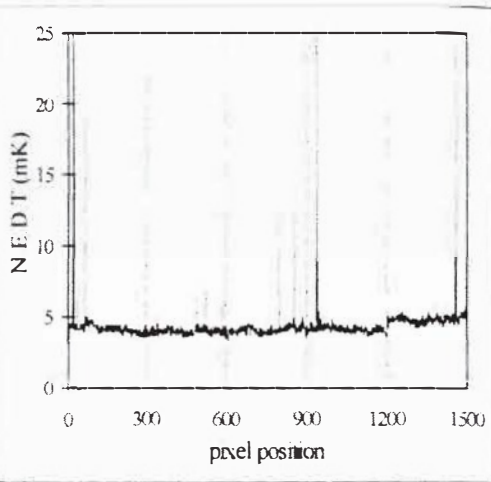


Figure 4: Spatial distribution of NEDT

Figures 5 and 6 show the response and detectivity histograms. These histograms were obtained after correction of the transmission of the cryostat window.

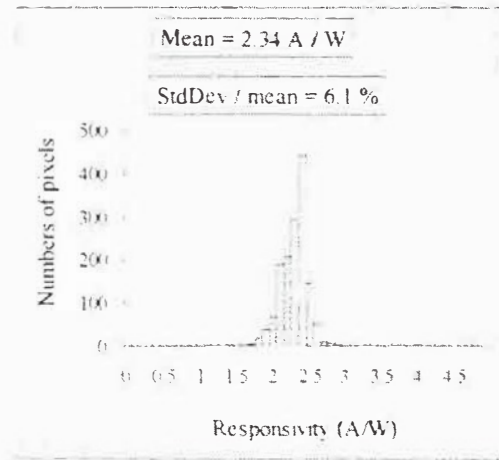


Figure 5: Responsivity histogram

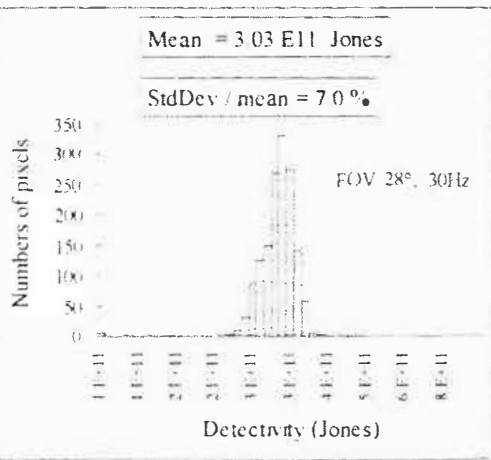


Figure 6: Detectivity histogram

The response value of 2.34 A/W corresponds to a detector quantum efficiency of 65%. The detectivity measured is very close to the BLIP value, the degradation observed is less than 10% and is essentially due to the reset noise of the readout circuit.

The table hereafter resumes the all performance values measured on the linear array

detector shunt impedance	> 100 GΩ
output rms noise (0.5-200Hz)	120 μV
detectivity	3 · 10 <sup>11</sup> J
responsivity	2.3 A/W
quantum efficiency	65 %
NEDT (half range)	4.3 mK
power consumption	1.5 mW
operational edge detectors	100 %
operational detectors (edge & center)	99.8 %
operational detectors (NEDT < 10 mK)	99.6 %

All these measurements show the excellent functionality of the 3-5 μm butted array. the level of performance is very close to the theoretical values and all the detectors located in the butting zone are operational.

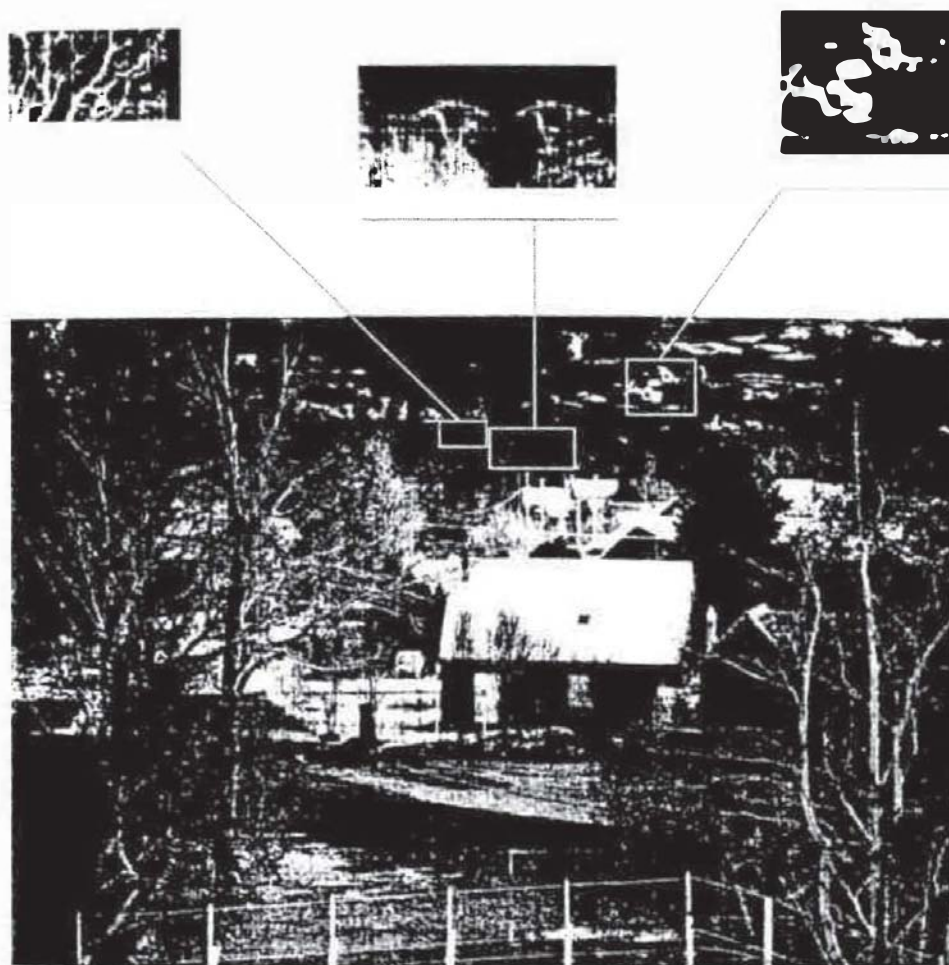


Figure 7 Infrared image using the 1500 element MWIR HgCdTe array Image format 1024 x 1500



A 1500 element butted array has been integrated into the ONERA instrument and first measurements have validated its design which conserves all the radiometric performance of the detectors.

Example of the images obtained on the ground in the vertical scanning mode is given in figure 7. This image with a definition of 1024 x 1500 pixels was obtained in 14-bit depth and the visualisation is shown in 256 levels. A geometrical correction for pixel realignment as well as a 2 points correction for gain and offset were carried out to generate this image. A local adjustment of the signal dynamics has been carried out in some arrays of interest (AOI) to bring out the overall radiometric capability of the instrument; it enables visualization of details such as electric cables and pylons, clouds and tree branches.

## 7. PERFORMANCE OF THE 1500 ELEMENT LWIR INCMOS BUTTED ARRAY

We present in this section the results obtained on a 1500 detector butted linear array operating in the 8-10  $\mu\text{m}$  range.

All the characterisations were carried out with an extended test pattern at 293K and 300 K. A 16 bit 100 khz digitizer was used to obtain acquisitions at pixel frequency with a 100  $\mu\text{V}$  LSB. The measurement of rms noise was made in the 0.6Hz - 400Hz band, the high value of 400 Hz being the frequency corresponding to the integration time.

The measurement conditions as well as the main characteristics of the component are given in the following table.

operating temperature	78 K
field of view	28°
cutoff wavelength	10 $\mu\text{m}$
frame frequency	400 Hz
pixel frequency	150 kHz
integration time	2.4 ms
charge handling capacity	1.3 $10^8 e^-$

The readout circuit operates in a skimming mode.

Figure 8 gives the NETD histogram measured for a charge stored in the pixel of  $9.3 \cdot 10^7$  electrons. This parameter is obtained for each detector by the ratio between the rms noise and the output response.

The mean value of 12mK is very closed to the theoretical Schottky value which means that there is no 1/f noise contribution. The overall detector operability is 98.3 %. For the edge detectors, high performances are obtained with less than 7 % of detectors presenting a NETD greater than 30 mK in the butted regions.

Figure 9 shows the influence of the adaptative bias function on the output level. This function allows to optimize the bias of the photovoltaic detectors and consequently to reduce the number of defects. Thanks to this correction, the number of defects with NETD  $\geq 100$  mK is reduced from 18 to 9 i.e. that the operability of the array passes from 98.8% to 99.4%.

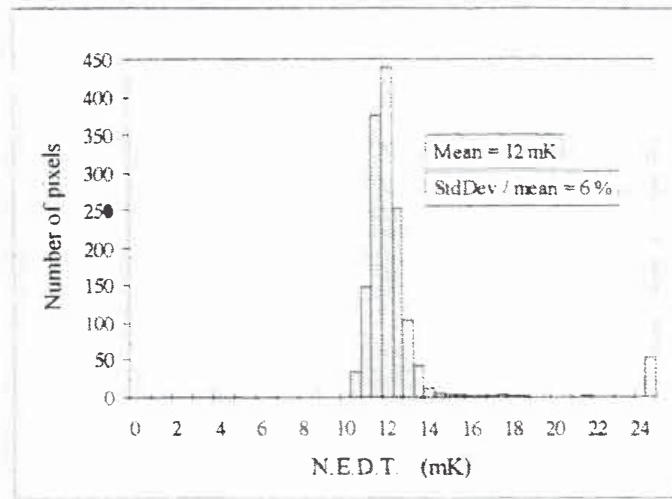


Figure 8: NEDT histogram of the 1500 element linear LWIR butted array

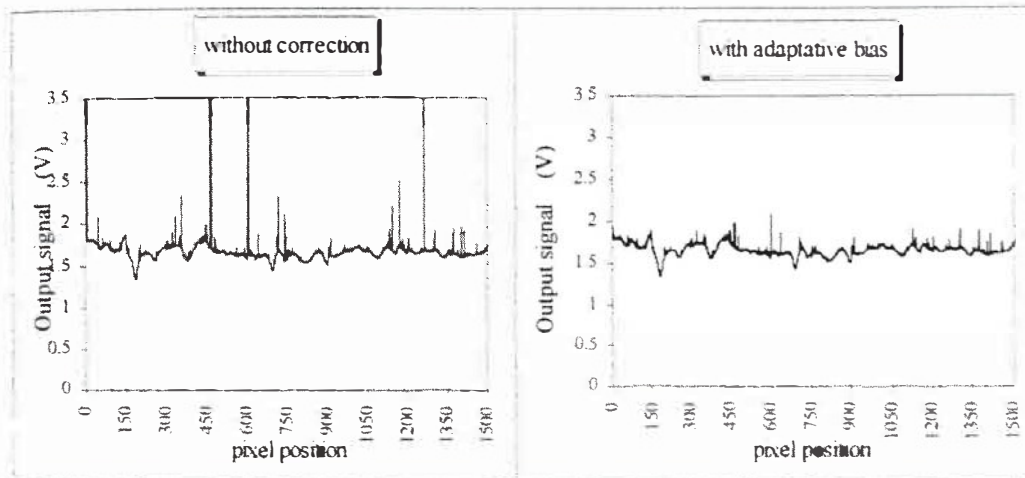


Figure 9. output level cartography (without and with the adaptive bias function)

The table hereafter summarizes the all performance values measured on the linear array.

detector shunt impedance	>1 GΩ
output rms noise	120 μV
responsivity	4 A/W
quantum efficiency	55 %
NEDT	12 mK
power consumption	4 mW
operational detectors (NETD < 100 mK)	99.4 %
operational detectors (NETD < 30 mK)	98.3 %

These measurements show the good functionality of the butted array the level of performance is close to the theoretical values and the operability is very good.

## 8. CONCLUSION AND PERSPECTIVES

Two long 1500 detector butted linear arrays with a modular architecture operating in the 3-5 and 8-10  $\mu\text{m}$  spectral ranges have been fabricated at LIR using specific butting technologies. Perfect functionality, very high performance close to the theoretical limit and excellent operability have been demonstrated by these prototypes. These results confirm the interest of a modular architecture for producing large complex focal plane arrays and demonstrate the feasibility of such devices.

Aerial experimentations are going to be undertaken by ONERA in order to qualify these prototypes

Obviously, this architecture is equally well-suited to other and more sophisticated focal plane arrays which may integrate functions of redundancy, pixel deselection or time delay integration (TDI). Moreover a modular approach derived from the present structure should be equally interesting for producing large butted 2D staring arrays.

With the level of performance and reliability attained by this butting technology we can now envisage the industrial technology transfer to SOFRADIR for the production of such arrays.

## 9. ACKNOWLEDGMENTS

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