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TDI-CMOS Image Sensor for Earth Observation

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1. ABSTRACT

The first Earth Observation satellites used linear sensors, which have a significant limitation in the signal that can be gathered in each pixel resulting in a limited ground sampling distance (GSD) in order to achieve the required signal to noise ratio (SNR). The solution to this was to use TDI (Time delay integration) detectors. The first generations of TDI detectors were based on CCDs, which can intrinsically operate in a TDI mode by moving charge within the detector at a rate corresponding to the movement of the satellite over the ground. The CCD technology used relatively large pixels (typically 10-13µm) with low line rate of typically around 10kHz achieving a ground resolution of down to 0.5m with very high SNR. More recent CCD TDI sensors can achieve line rates of up to 30kHz with pixels as small as 7µm but the interfaces become extremely complex and power dissipation is high. Improvements to satellite technology means that a higher resolution is now achievable and this requires higher line rates, over 30kHz and pixel sizes significantly below 7µm as well as more complex sensors with higher numbers of multispectral lines to give improved spectral data. In order to achieve all of these requirements the use of a CMOS sensor with on chip digitization become essential.

The first CMOS approach was to carry the TDI functionality using digital summation. This approach quickly demonstrated limitations in terms of line rate and power consumption as the entire sensor has to be read for every line on the ground that is sampled. More recently CMOS technology has matured the charge domain CCD approach with comparable electro-optical performance to CCDs while offering higher speed, smaller pixel pitch and high level of integration.

This latest technology step has also considerably eased the integration of the sensor into the satellite, opening new opportunities to produce focal planes at significantly lower cost with much reduced power dissipation, size and weight. The challenge has been to establish a CCD on CMOS technology that can obtain a similar full well capacity and charge transfer efficiency (CTE) performance to CCDs. This CCD on CMOS technology has now reached the point where the performance is comparable to CCDs but with very much lower operating voltages.

This paper will present the evolution of earth scanning image sensors with a focus on the latest TDI CMOS technology including the recent results obtained with the latest CMOS technology using TDI in charge domain approach. These results will include FWC, CTE, radiation performance as well as results from very high speed, up to 3.6Gbps output stream, and highly integrated readout circuitry.

Finally we will provide details of new devices that will provide performance that would not have been possible with CCDs.

2. CCD STRUCTURE

The pixel architecture used for TDI-CMOS charge domain (or qTDI) is represented in Figure 1. It is a 4 phase CCD structure with minimum poly-poly gap (0.25µm). The pixel is bi-directional with identical output ports at either end of the CCD structure. This structure is based on a buried channel implantation to achieve good charge transfer efficiency (CTE) and to minimize post radiation degradation as seen with surface channel approach [1].

The clocking of the CCD phases is overlapping as shown in Figure 2. The transfer direction can simply be changed by swapping two of the clocks. This feature is accessible via an SPI interface. Gate voltage and clock slew rate are optimized for best full well capacity and CTE trade-off.

The clock generator and drivers are embedded in the chip greatly simplifying the integration of this detector. Note that careful lay out technics are used to obtain correct clock slew rate and avoid IR drops due to current demand during switching activity.

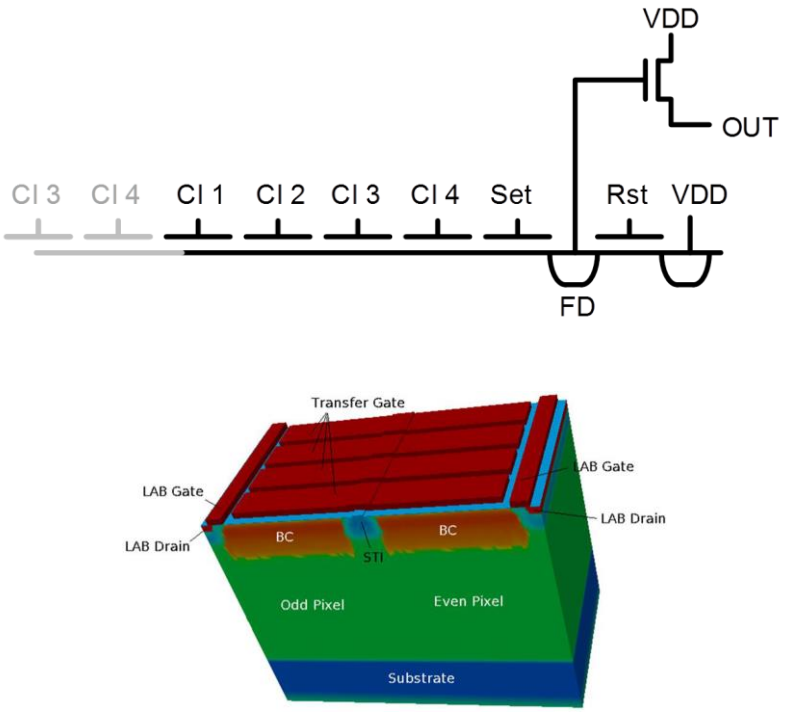

Figure 1 Pixel schematic and 3D structure.

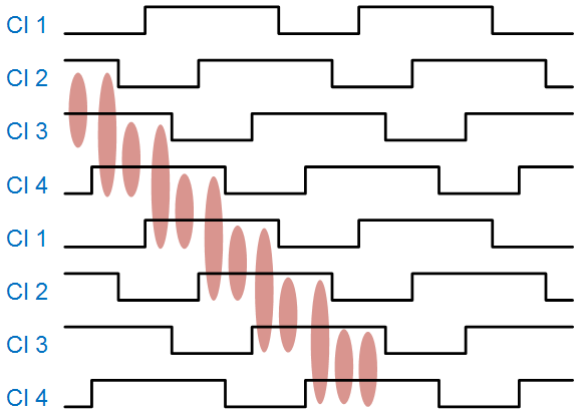

Figure 2: CCD structure phase clocking.

3. PROTOTYPE EVALUATION

A prototype, see Figure 3, was developed to test CCD structure variants with 2 pixel pitches of 5 and 10 µm. This prototype was designed to not only prove the pixel technology but also a periphery to support high line rate up to 300klines/s. The image area is composed of a single TDI-CCD structure of 4096 columns with 256 or 64 TDI stages depending on the pixel pitch. In order to achieve this line rate of up to 300 klines/s a very fast single slope 12 bits ADC technique has been developed and implemented. The 12 bits conversion is achieved in 0.9µs. The classic single slope ADC architecture was modified to work around a counter generating eleven Gray code bits and three phase-shifted clocks providing 12 bits output (see Figure 4) in total at very high line rates:

- Phase shifted clocks are used to add one bit of resolution, working around speed limitations of clock distribution network and CMOS process.
- Counter-bits are distributed in low swing differential fashion. Regenerative latches in the columns convert the signals to full CMOS swing.
- Using clocks running at a maximum clock frequency of 600MHz an effective count-rate of 4.8 GHz is achieved hence 12 bits conversion in less than 0.9µs.

The complete column readout path is illustrated in Figure 5.

The data resulting of the image conversion is then sent to a gigabit transmitter (GTX) composed of a serializer working in double data rate mode (DDR) at 3.6GHz and a CML (3.6Gb/s) data driver. A high speed CML output driver has been selected to minimize the number of output ports to simplify the interface to the data capturing device. Input signals such as clock, integration control and SPI interface use LVDS format.

The CCD-structure clock drivers require attention and floor planning, see Figure 6:

- Gate Drivers repeat every 64 columns
- Vertical strapping used to connect CCD clock signals
- Array divided in equal sections of 64 rows.
- Shielded isolation rows along the top and bottom side of the array.
- Unselected stages are clocked in reverse direction

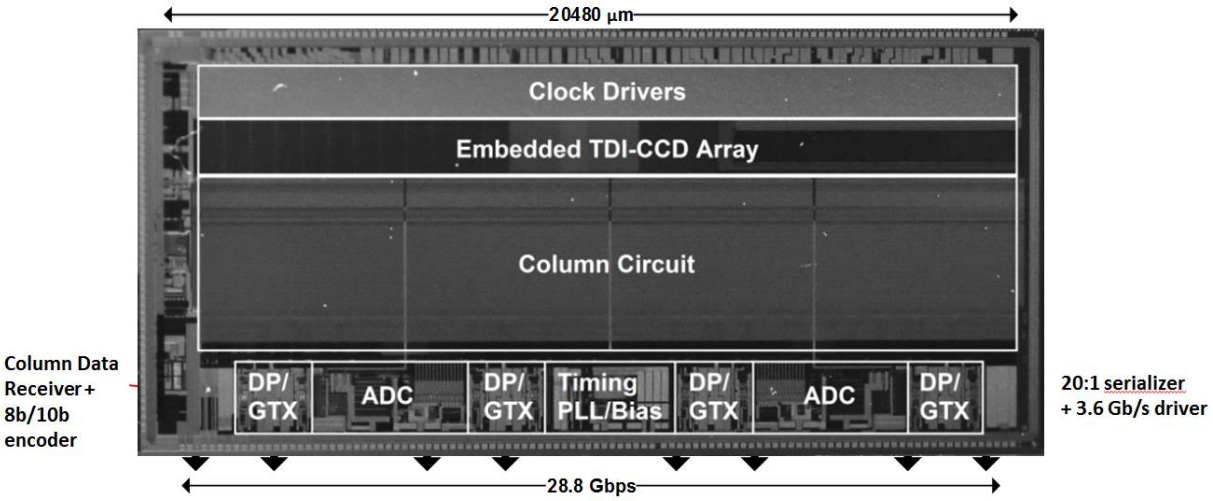

Figure 3 Die design prototype

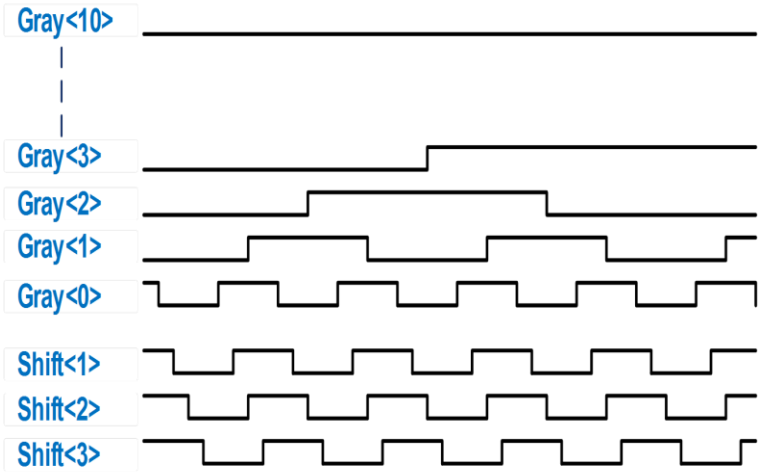

Figure 4 Example of timing access to the sensor CIS125.

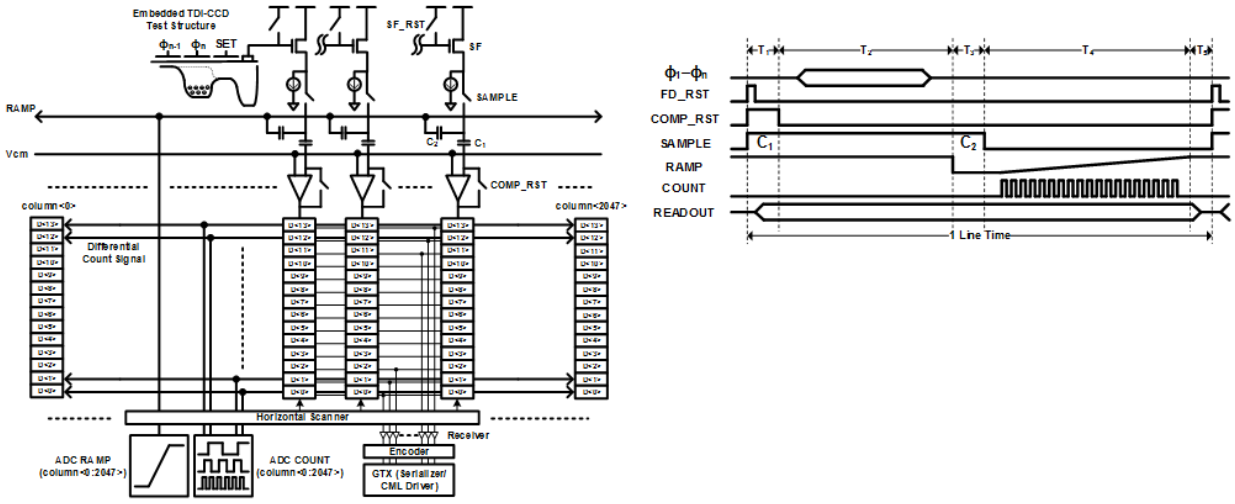

Figure 5 High speed ADC readout diagram and timing.

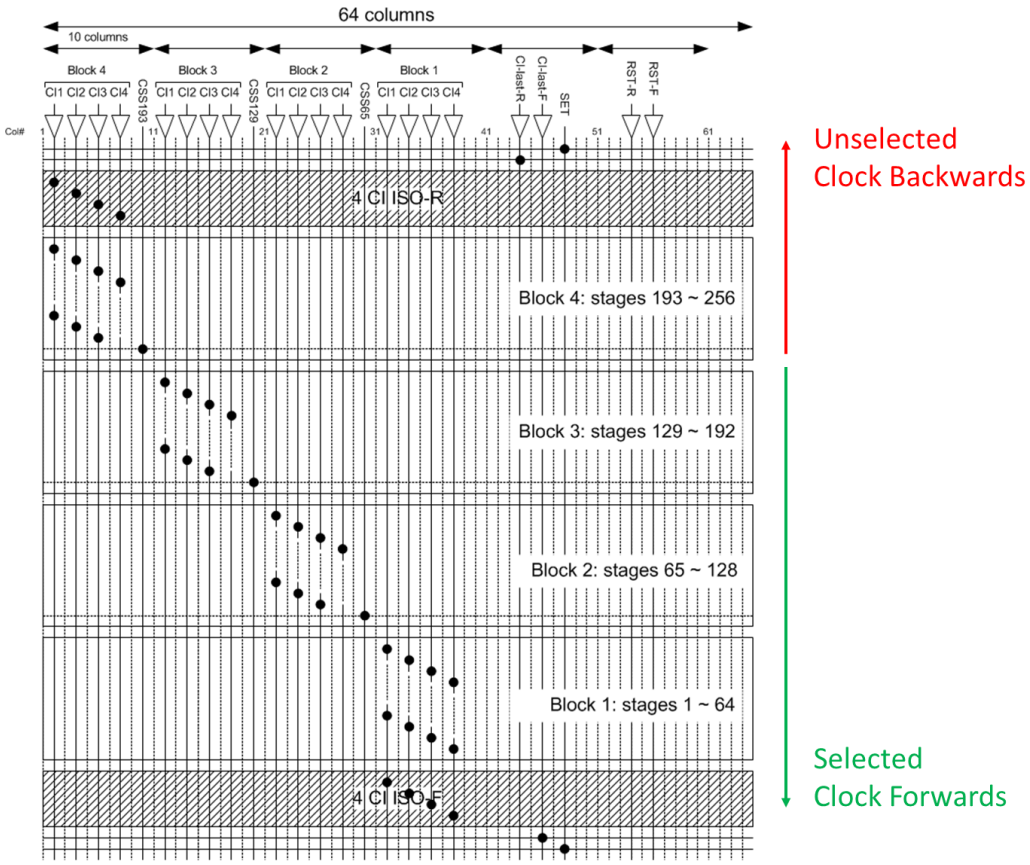

Figure 6 CCD structure phase clocking.

4. PROTOTYPE DEVICE EXPERIMENTAL RESULTS

4.1 Results summary

Table 1 summarizes the obtained results. The results demonstrate good performance and readiness for use for space mission.

Feature	Unit	Target	Measured
Pixel pitch	µm	5 & 10	5 & 10
Vertical resolution	Pixels	256	256
1D stitchable		Yes	Yes
Bi-directionality		Required	Demonstrated
Stage selection		64/128/192/256	64/128/192/256
CTE / gate		> 0.99998	> 0.99999
FWC - 5 µm pixel	electrons	> 20 K (Non-AB)	> 30 k (AB)
Noise Floor	electrons	< 15	12

Anti-Blooming (AB)	×Sat	> 100	***Note 1***
Max line rate	kHz	> 300	270 confirmed *Note 2*
Dark Current @ 25°C	nA/cm^2	< 10	3.7
Non-linearity	%	< 2	< 2
Peak QE (FSI)	%	≥ 40	> 45 @ 650 nm
ADC	bit	12	12
Data streaming - Format - Interface		8b/10b encoded 8 ports 3.6 Gbps	8b/10b encoded 8 ports 3.6 Gbps

Table 1: Prototype summary results.

Note1: AB demonstrated, actual performance to be quantified

Note 2: Read-out chain limitation resolved

4.2 Electro-optical performance

The implementation of good CCD structure in CMOS represents several challenges of which the two mains ones are obtaining good CTE and high enough full well capacity. In that respect and compared to CCD the limitations of CMOS technology to be overcome are non-overlapping poly gates and lower supply voltages. The former affects the CTE and the later the FWC. In addition and similar to CCD technology a surface channel CCD structure although giving higher full well will suffer from high CTE degradation end of life (EOL) worsening drastically MTF performance. This is because trap generated at the silicon surface will trap and release electron at different clock phases. Hence all the CCD structure pixels use buried channel architecture despite the loss of Full Well. An advantage of the buried implant is that it reduces the potential pockets of poly-poly gap (0.25µm). In order to overcome the lower supply voltage of CMOS technology negative supplies are used to increase the potential across each pixel. It can be noted that summing in the digital domain two of the CCD structure, also called sub-TDI arrays is recommended to increase the signal noise ratio. This is because while the total charge is added in a linear fashion the noise is added in root square fashion only.

A summary of the main results are given below and can be found in more details in [1]. On a 5µm pitch CCD structure with anti-blooming a FWC of 30ke- was measured with a CTE better than 0.99999. The signal non-linearity achieved is less than 2%, while the dark current performance is 3.7 nA/cm^2 with a temperature doubling factor of 9.5°C. The Arrhenius plot indicates an activation energy (E_a) of 0.6eV. This corresponds to half the silicon band gap confirming that the dark current source is the conventional Shockley-Read-Hall (SRH) mechanism. The charge conversion efficiency graph shows a pixel conversion gain of 35µV/e-. This gain is designed to optimise noise floor versus full well and hence dynamic range.

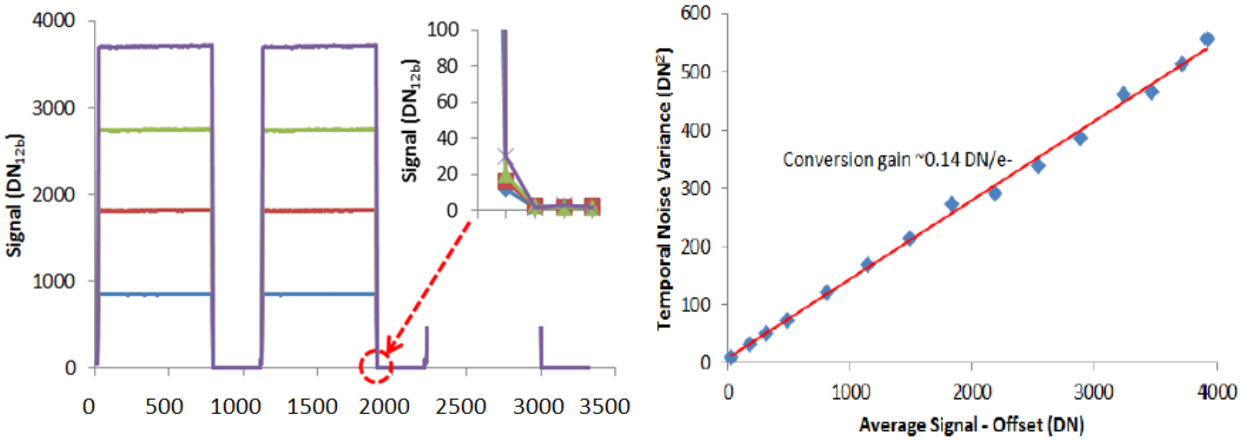

Figure 7 Left CTE measurements and right Photon Transfer Curve.

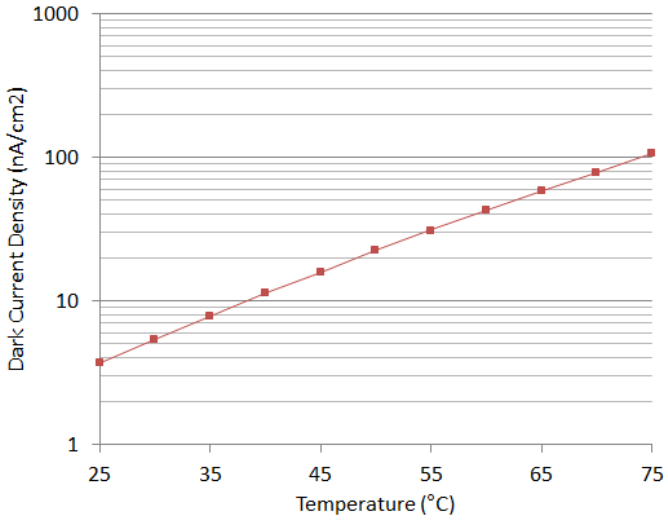

Figure 8 Dark current.

4.3 Radiation

The radiation immunity or degradation model is a key aspect of validation of a new technology. In the context of the qTDI detector two aspects matters: the CCD structure behaviour with Gamma and Proton and the readout periphery immunity to Heavy Ion. Results obtained on these two aspects are shown below.

4.4 CCD structure

For the CCD structure the concerns are mainly around two parameters, dark current (including bright pixel) and CTE performance degradation when subject to Gamma and proton radiation. The results [4] below show a good behaviour with acceptable results for a flight mission.

The Gamma radiation increased the dark signal of the Non-Anti-bloomed (AB) split by a factor 2 at 30krad while the AB split was more affected (x2.5). This is explained by the fact that AB split has less STI and less active area but has more gate edges and poly gaps (Non-continuous poly gates). A similar observation is made after the proton irradiation, see table for details. The higher increase for the AB splits is also explained by the higher level of gate edges.

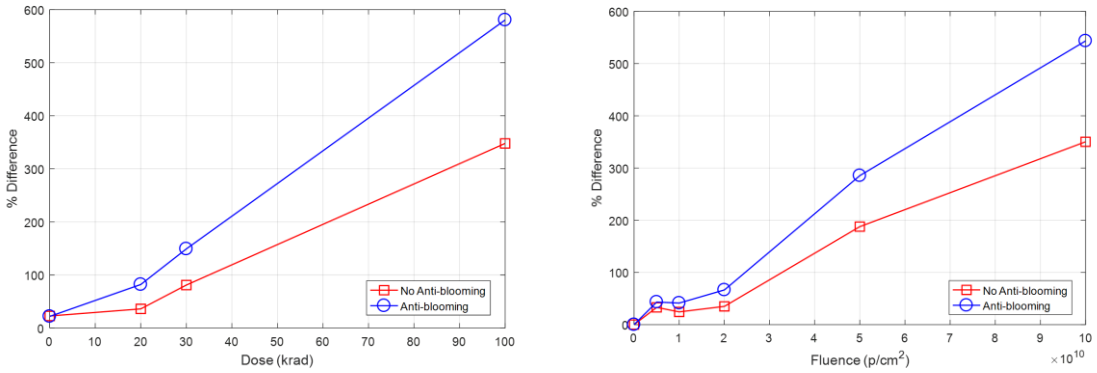

Figure 9 Post radiation dark current: Left is post Gamma and 7 days room temperature anneal; right is post Proton and 14 days room temperature anneal.

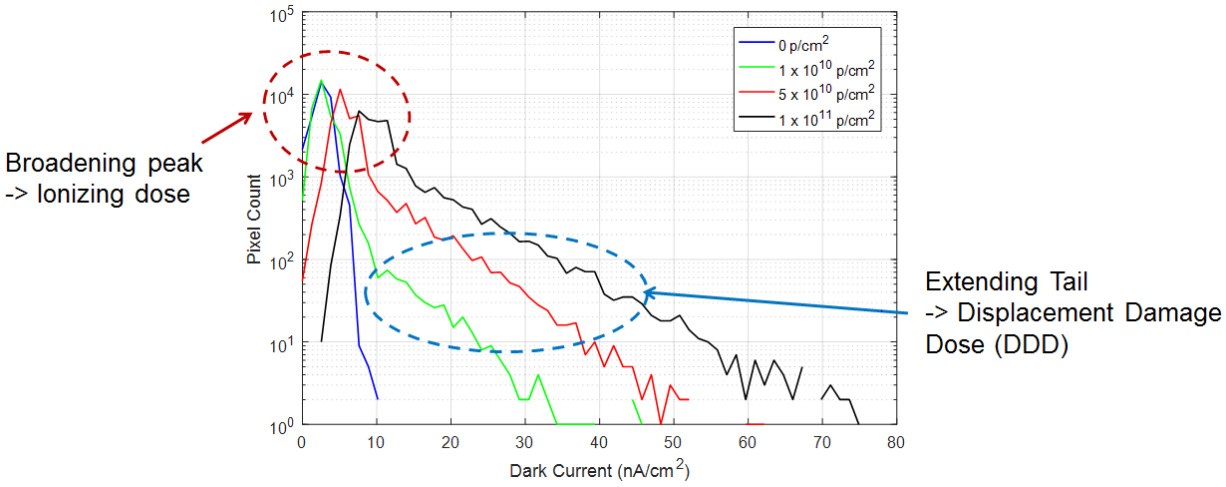

Figure 10 Bright pixel post proton and 14 days room temperature anneal.

	Pre-radiation	Post Gamma 30krad	Post proton - 5x1010 p/cm2
Without AB	3-4nA/cm^2	< x2	<x3
With AB	3-4nA/cm^2	~x2.5	<x4

Table 2 Dark current summary at 30krad and 5x10^{10} p/cm^2 Proton exposure.

The results below show a very small and similar CTE degradation of both the AB and non-AB versions of the prototype device with Gamma and proton up to doses that would be expected in typical space based applications

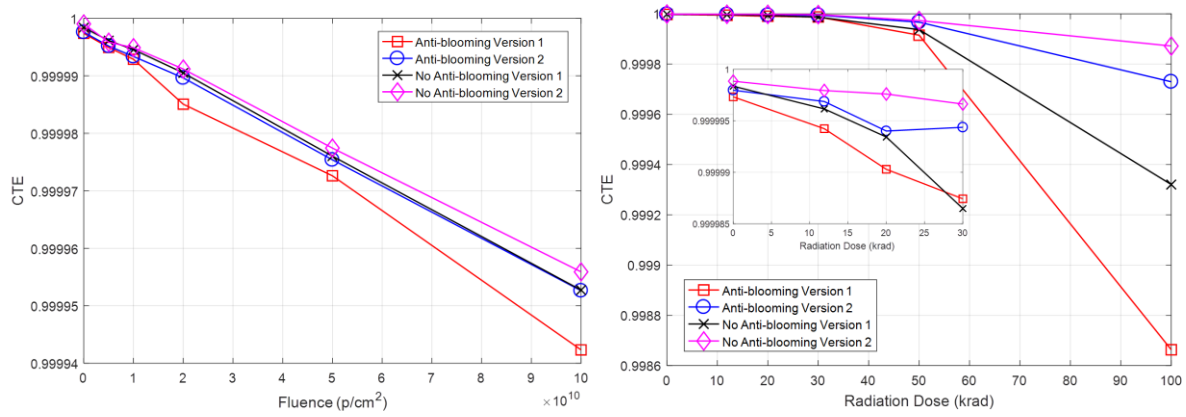

Figure 10 CTE versus Proton fluence (left) and Gamma dose (Right).

Single Event Effect (SEE)

Usually, the SEE is categorized in:

- Non-destructive
  - Single event upset (SEU) – change of logic state in memory element.
  - Single event transient (SET) – transients in circuit that lead to erroneous data being captured.
  - Single event functional interrupt (SEFI) – temporary loss of device functionality (for an imager of this simplicity, this is caused by bus contention).
- Potentially Destructive
  - Single event latch-up (SEL) – a parasitic thyristor causes circuit lockup or catastrophic failure.

Teledyne has developed design rules and layout rules that have secured several projects such as MTG or METImage giving high immunity to heavy ion. These results have been reported in details at the ICSO conference 2016 and below is a summary table.

	LETth ($MeVcm^2mg^{-1}$)	Mission rate (day^{-1})	Reliability over 8.5 years (%)	Comments
SEL	> 67.7	< $2x10^{-6}$	99.2	This worst case as no latch-up was actually observed
SEU rad-hard register	65	< $4x10^{-12}$	99.9999	Sequencer, timing and readout control
SEU low power register	19	< $1x10^{-8}$	99.996	Serial programmable interface

Table 3 MTG-FCI results 3.

5. NEXT ACTIVITIES

The technology described in this paper is now being used to make a prototype full sized TDI CMOS image sensor called the CIS125 in a program funded by the UK Space Agency (CEOI). The architecture developed is shown Figure 11. This qTDI detector is composed of 4 panchromatic (PAN) bands and 8 multi-spectral (MS) bands. The configuration reported here is optimised for the CEOI program and each PAN and MS are composed of sub-TDI bands (A&B) that enhance the full well by adding digital summation to the charge domain performance. The PAN and MS number of TDI lines were carefully chosen to optimise application needs versus silicon area. Each sub-TDI needs to be read out separately and therefore needs its own conversion. This is the equivalent of reading out 16 independent bands.

This sensor is a stitched device of 16k columns for the PAN and 8k columns for the MS. The pixel is 5µm and 10µm for the PAN and MS respectively, see Table 4. The high speed ADC per column described earlier allows a line rate of up to 14kHz if all of the sensor lines and sub lines are read. A single read path is shared between all bands enabling the implementation of a maximum number of bands without the need of 2D stitching technology and optimising power consumption.

The number of TDI stages per bands are selectable as follow:

- Each sub-TDI PAN array can be programed in the following steps: 1, 4, 8, 16, 24, 32, 48 and 64.
- Each MS array can be programed (independently for each MS) in the following steps: 1, 2, 4, 8, 12, 16, 24 and 32.
- For the secondary, shorter sub-TDI sections (PANs with 32 and MSs with 16), will mirror the options of the primary ones, for the available number of lines.

This sensor will be made with a 0.18µm Imaging CMOS process using thick and high resistivity epitaxial silicon. The device is also back-illuminated to improve fill factor and it will be thinned (using Teledyne-e2v process) to optimise QE versus MTF. To enhance further it performance an Anti-reflection coating will be deposited as well as black-coating between channels to avoid straight light effects.

CIS125 is designed as a modular platform to enable to adapt to a wide range of configuration with lower risk associated to new development.

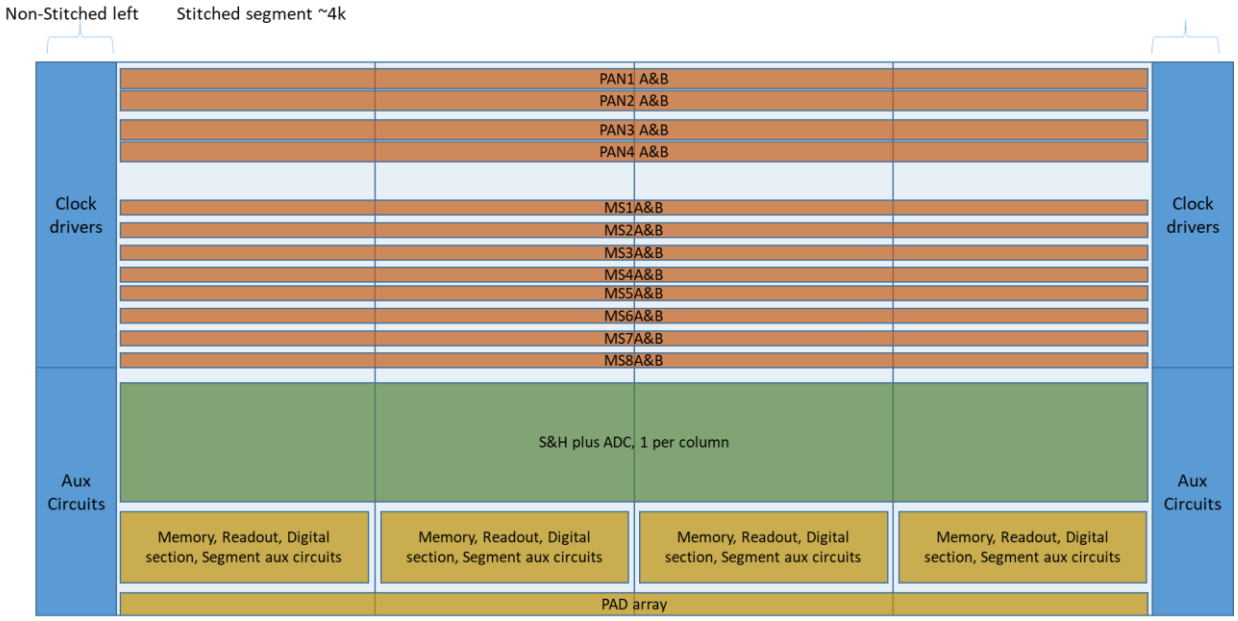

Figure 11 Sensor Architecture

Pixel count		Pixel size (µm)		Line rate (kHz)		Delivery
PAN	MS	PAN	MS	PAN	MS	
16k	8k	5	10	14	7	2019

Table 4 Configuration for CEOI program.

6. SUMMARY

A TDI-CMOS sensor for high resolution earth observation has been presented:

- Innovative CCD-structure enables charge domain transfer for high resolution.
- The prototype demonstrates good electro-optical performance with very high line rate enabling multi-bands application at high line rates:
    - A 12 bits single slope ADC with conversion of 0.9µs.
    - High speed data output drivers (CML)
    - Embedded phase driver carefully implement to achieve fast rise and fall time despite the loading.
- The prototype has also demonstrated compatibility between high performance and high level of integration enabling easier integration at system level without compromise on image quality.

In this paper has also presented the performance of the CCD structure used and demonstrated high TRL level:

- CTE of 0.99999 and Full Well of 30ke$^-$ for 5µm pixel pitch and high line rate.
- Other performance such as dark current or linearity been within expectation.
- Post radiation Gamma and Proton performance and especially CTE and dark current having a reasonable degradation and therefore acceptable for flight.

This technology has now reached a maturity where full sensors are being design for flight applications and example is give showing the type of architecture that is possible in a full sensor design

7. References

[1] Hyun Jung, Lee et al., “Charge-Coupled CMOS TDI Imager,” Image Sensors Workshop (2017)

[2] Tsung-Hsun Tsai et al., “A 12-bit, 0.9µs Single Slope ADC for Embedded TDI-CCD and CMOS Line-Scan Image Sensor,” Image Sensors Workshop (2017)

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[5] Pratlong J. et al., “CMOS Sensors for Atmospheric Imaging,” ICSO conference (October 2016).