Special Section Guest Editorial: Novel Patterning Technologies II

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We are pleased to offer the second Special Section on Novel Patterning Technologies. Part of the appeal of this section is that it highlights both lithographic and patterning technologies that are relevant for the fabrication of devices both in the semiconductor mainstream and technologies that are just becoming important to our community. As an example, nanoimprint lithography is being targeted for advanced memory devices but has also been used to fabricate diffractive gratings, metasurfaces, and wire grid polarizers. In our community we tend to think about lithography as technology that is critical to extending device roadmaps through pitch reduction methods. However, lithography also applies to back-end packaging steps, and new tools and processes are essential for extending device roadmaps. New patterning methods that enable high quality, low defect, and cost effective pattern transfer are needed to complement lithography improvements.

There are seven papers in this section, which touch on the topics described above and can be divided into three rather diverse categories: nanoimprint lithography (NIL), circuit board patterning, and pattern transfer using metal-assisted chemical etching.

For NIL, there are five papers: three from Kioxia, one from Canon and one from Canon Nanotechnologies. The papers from Kioxia have a common theme of improved productivity. Nakasugi et al. discuss the feasibility of printing multiple fields with a single shot as a means of increasing tool throughput. In this work, an imprint mask with a field size of 46 mm × 28 mm is used to target an output of 160 wafers per hour. Okabe et al. apply a gas permeable spin on carbon underlayer in order to promote the diffusion of gas present between resist droplets and minimize resist fill time. Finally, Iwasaki explores the use of spin-on resists to improve productivity and also applies various methods to further reduce defectivity.

The Canon and Canon Nanotechnologies papers have a computational modeling theme. Seki et al. introduce computational models and present a NIL simulator which applies fluid structure interactions to understand resist drop coalescence and resist fill. The simulator is able to predict resist spread time, identify filling hot spots and can also predict residual layer film distribution. Roy et al. have developed models to account for imprint force and tip/tilt of the imprint head relative to the wafer as a means to achieve a more stable imprint process and reduce overlay errors.

Rao et al., from the Birla Institute of Technology and Science and the U R Rao Satellite Center, introduce a patterning process for high density interconnect printed circuit boards and apply a digital micromirror array to a liquid photosensitive resist to achieve improved circuit patterning. The methods described are relevant for military and aerospace applications.

Finally, Van Minh et al., from the Hanoi University of Science and Technology, Vietnam Maritime University, FPT University, and the Vietnam Academy of Science and Technology, combine the use of silica nanoparticle lithography and metal-assisted chemical etching (MACE) to fabricate dense arrays of silicon nanopillars.

This collection of papers would not have been possible without the effort of all of the authors and reviewers, and we are grateful for their time and effort. We are very aware that reviewers need to set aside time from their day-to-day activities, and their dedication to the reviewing task provides a valuable service to our community and also helps to promote technology development. In addition, we appreciate the professional guidance of the JM3 editorial team. Their help made the entire review process run seamlessly. Finally, we are thankful for the advice and inputs of JM3 Editor-in-Chief Harry Levinson. We hope you enjoy the contents of this section and invite your comments and feedback.