Design and fabrication of compact nonblocking 4×4 optical matrix switch on silicon-on-insulator by anisotropic chemical etching

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Abstract. A folding nonblocking 4×4 optical matrix switch in simplified-tree architecture was designed and fabricated on a silicon-on-insulator wafer. To compress chip size, switch elements (SEs) were connected by total internal reflection mirrors instead of conventional S-bends. For obtaining smooth interfaces, potassium hydroxide (KOH) anisotropic chemical etching of silicon was employed. The device has a compact size of 20×3.2 mm^2 and a fast response of 8±1 μs. Power consumption of 2×2 SE and excess loss per mirror were 145 mW and −1.1 dB, respectively. © *2005 Society of Photo-Optical Instrumentation Engineers.*
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1 Introduction

Optical switches play an important role in many applications, such as optical cross connection (OXC) and optical add-drop multiplexing (OADM). Nowadays, silicon-on-insulator (SOI) technology has attracted much attention in these applications due to its perfect compatibility with current microelectronics technology. Some optical switches with fast response (less than 10 μs) have been realized on SOI wafers.[1] These switches, however, only have a small port count, such as 1×1 and 2×2. The matrix switch will suffer from exorbitant length, serious bend loss, and inevitable intersection crosstalk if switch elements (SEs) are connected by conventional S-bends. In this letter, a folding large-scale optical matrix switch was demonstrated on SOI by wet chemical etching. To compress the chip and reduce bend loss as well as crosstalk efficiently, the light circuit is folded by connecting SEs by mirrors instead of S-bends.

2 Design

Simplified-tree architecture, which has advantages of low crosstalk and small path dependence in propagation loss, is used for the nonblocking 4×4 matrix switch shown in Fig. 1(a).[2] Unlike the conventional structure in which SEs are connected by S-bends, total internal reflection (TIR) mirrors are employed in pairs to connect SEs in our novel folding matrix switch [see Fig. 1(b)].

An oriented (100) SOI wafer with a 5-μm top silicon layer and 1-μm buried silicon oxide was used. The device was fabricated by potassium hydroxide (KOH) anisotropy etching of silicon rather than dry etching, such as reactive ion etching (RIE). The waveguides with a trapeziform section, whose bottom angle is 54.74 deg, are along the ⟨110⟩ crystalline direction of the wafer, and underetched vertical walls along the ⟨100⟩ direction do duty for mirrors. There is a well-defined 45-deg angle between the ⟨100⟩ and ⟨110⟩ directions. In addition, the (100) crystalline plane is naturally perpendicular to the surface. Therefore the anisotropy chemical etching tends to be a quasi self-aligned method.

Figure 1(c) shows the structure of a 2×2 switch with a multimode interference (MMI) splitter and combiner. Thermo-optic (TO) phase shifting is utilized because silicon has a high thermo-optic coefficient and high thermal conductivity. Except MMI, almost all waveguides work in single mode. Width and etching depth of the single-mode waveguide are designed to be 5 μm and 1.5 μm, and the refractive indexes of the fundamental mode for quasi-TE and quasi-TM cases are 3.49579 and 3.49556, respectively (n_{Si}=3.5, n_{SiO2}=1.45, λ_0=1.55 μm). The calculated optimum length of 30-μm-wide MMI is 5330 μm. The MMIs are connected by two straight phase-shifting arms instead of S-bends to shorten the length of the device. Trenches are introduced to avoid mode coupling and isolate heat transfer between the two arms.

Recently, a TIR mirror with low loss of −0.5 dB has been realized on a SOI substrate by wet chemical etching.[3] Masks of the mirror and waveguides used here are shown in Fig. 1(d). The first mask defines waveguides and a trigonal area. The second mask is used to open a window in the trigonal area for mirror facet etching. The dashed line is the final position of the mirror facet to be controlled by etching time.

3 Experiment and Results

We have fabricated the matrix switch by KOH anisotropic etching. The device has a compact size of 20×3.2 mm^2 compared with a silica-based matrix switch whose size is about 25×65 mm^2.[4] Using a thinner top silicon layer or paired interference in MMI will diminish the device size more. For example, the size of the switch will reduce to about 4×3.2 mm^2 when the top silicon layer is 3 μm.

The roughness of the etched (100) crystalline plane, which acts as a mirror, testified from an atomic force microscope, was about 1.5 nm. The result is much smaller than ~20 nm for RIE. Considering that the etching speed of the waveguide sidewalls [(111) plane] is much slower than that of the (100) plane, the roughness of the sidewall should be smaller than 1.5 nm. A scanning electron microscope (SEM) micrograph of the mirror shown in Fig. 2 indicates that an excellent mirror with a smooth and vertical facet has been realized.

A switching speed of 8±1 μs was obtained (at 25°C, λ_0=1.55 μm), which is much faster than those of silica and polymer waveguide switches. The switching power con-

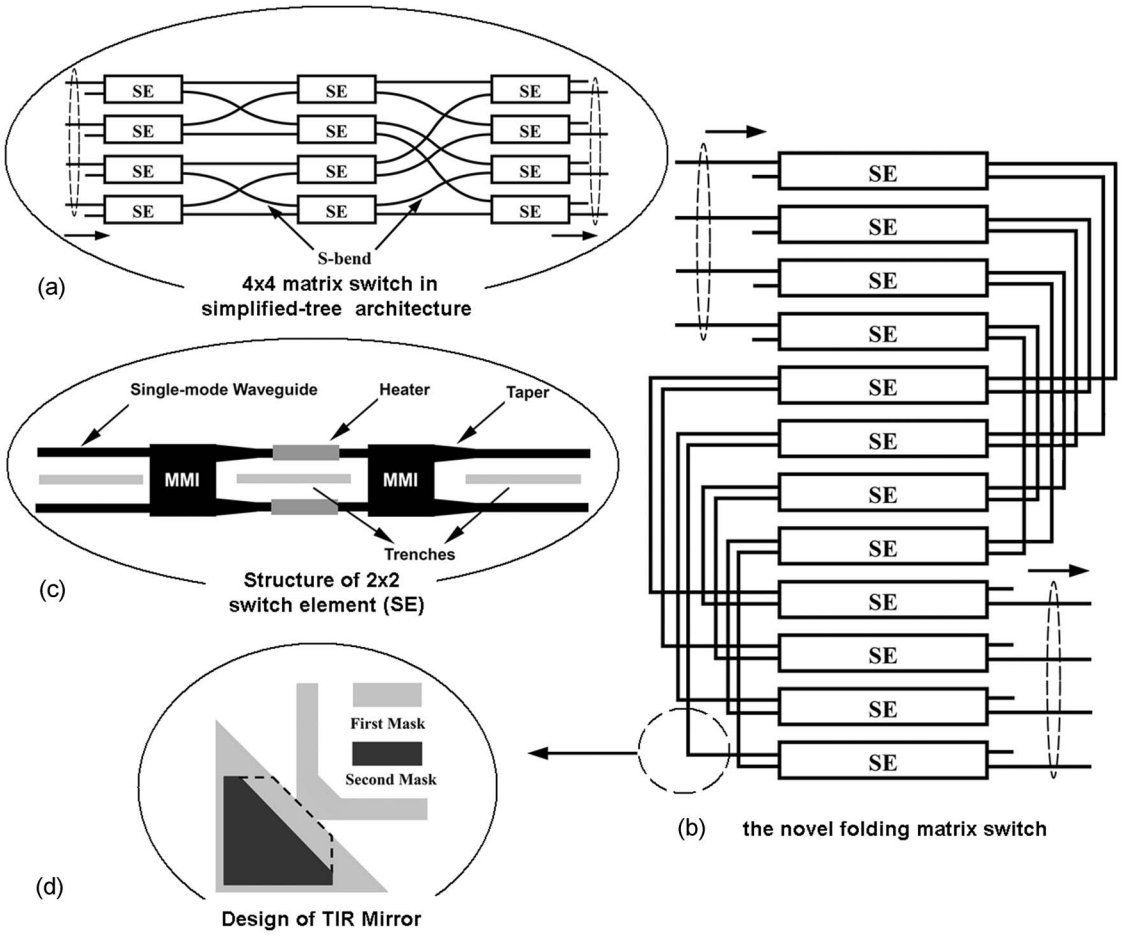

Fig. 1 Design of the novel folding matrix switch: (a) conventional 4×4 matrix switch in simplified-tree architecture; (b) layout of novel folding matrix switch; (c) structure of SE; (d) design of TIR mirror.

sumption of SE is 145 mW, which is much lower than the reported results in Ref. 1 due to the introduction of the blocking trenches.

The measured excess loss of the device is about -10.7 dB compared with that of a straight waveguide. Excess losses of individual components were measured of -1.1 dB per mirror and -2.4 dB per SE, respectively. The TIR mirror has an excellent verticality according to the SEM photos. The vertical tilt angle is measured to be less than 1 deg. This tilt introduces about -0.5 dB loss per mirror. Therefore, we think the value of 1 deg is the tolerance for a matrix switch. The reflectivity of the mirror is also sensitive to the offset between the ideal and experimental positions of the reflective facet. It is not easy to control all facets etched to their ideal positions synchronously because of photolithography errors. Nevertheless, this problem can be solved efficiently by a self-aligned method.[5] The measured polarized dependent loss (PDL) of the mirror can be ignored, and the value of SE is about -0.56 dB due to asymmetry of the layout of the metal electrodes.[1]

The crosstalk and extinction ratio of the device are about -18 and 17 dB, respectively, which are approximate to those of each SE.[2] These values, as well as the excess loss, were degraded by a ±0.5 μm thickness unevenness of the wafer and fabrication error. The characteristics of SE will benefit from deeper etching and wider MMI because more modes will be excited.

4 Conclusion

A folding nonblocking 4×4 optical matrix switch has been designed and fabricated on a SOI wafer. In this novel de-

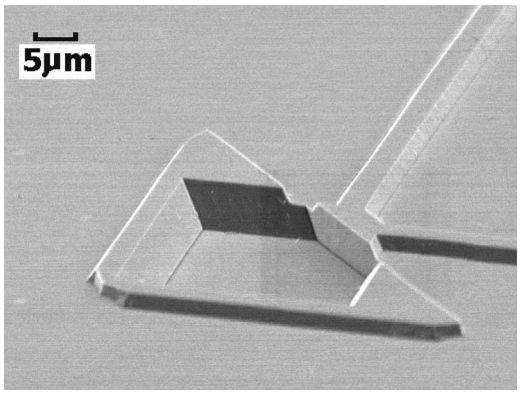

Fig. 2 SEM photo of TIR mirror.

vice, SEs were connected by TIR mirrors instead of conventional S-bends. To obtain smooth interfaces of the waveguide and vertical mirror facet, anisotropic chemical etching of silicon was employed. As a result, the device has a compact size of 20×3.2 mm^2 and a fast response of 8 ± 1 μs. Power consumption of each SE and excess loss per mirror were 145 mW and -1.1 dB, respectively.

Acknowledgments

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