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Chris Mack

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Thirty years ago, when I began working in lithography for semiconductor manufacturing, the bellwether of our industry was DRAM. Resolution was defined by the smallest DRAM half-pitch, and our technology nodes were named after DRAM densities. DRAM costs often determined the affordability of a personal computer, and everyone wanted more memory. By the 1990s, microprocessors began to dominate the business, and the frequency wars pushed gate length as the most important feature size (smaller gate lengths meant faster transistors). Logic gate lengths shrank faster than pitch, and two resolution measures were needed: minimum feature size and minimum half pitch. Nodes came to be named after the feature size.

About ten years ago, however, Dennard scaling (that wonderful bit of physics that said a smaller transistor was both faster and used less power) slowed to a halt: we could no longer shrink supply voltages, a necessary part of the scaling physics. This meant that a shrinking a transistor would increase its power consumption rather than lower it. Chip frequencies stopped growing, and power consumption became the new metric of success for chip performance. Gate lengths stalled at about 40 to 50 nm for several generations, and once again minimum half-pitch became the dominant measure of lithography performance. Unfortunately, technology node names came under the dominion of the marketing departments of the semiconductor companies and became disconnected from both minimum feature size and minimum half-pitch. Today the node names are names, not numbers.

Along the way, a new device technology came on the scene: flash memory. For flash, density is determined by a simple cross-bar structure of bit and word lines, so that the minimum half-pitch of a regular array of lines and spaces is the measure of lithographic success. And the business success of flash memory has resulted in ever greater densities, first in digital cameras, then in smart phones and many other mobile devices. In a typical smart phone today, the cost of the microprocessor is about half of the cost of the flash memory in that phone.

Flash has pushed resolution faster than DRAM and logic, and is the new industry bellwether. Flash became the first to use 193-nm immersion lithography in manufacturing. Flash was the first to employ pitch-division double patterning (the sidewall spacer type, where each edge of the original lithographic feature is turned into a narrow line), breaking the 78-nm pitch barrier of immersion single patterning. DRAM followed later with double patterning, and logic is about to employ pitch division for the first time this year, a full two or three generations behind flash.

Flash is about to lead the industry in new directions again. Without a practical EUV lithography option, flash manufacturers will likely use quadruple patterning (sidewall double patterning applied twice) to bring the minimum half-pitch below 19 nm by next year or so. But conventional flash transistors can only scale so far. Below about 15 nm in width, the floating-gate transistors that make up the flash memory array no longer store enough electrons to be reliable. Flash manufacturers are working hard to bring a new architecture to market: the vertical (or 3D) NAND flash transistor.

Vertical NAND tips the standard transistor by 90 degrees. Instead of drain, gate, and source side by side along the surface of the wafer, the source is stacked on top of the gate, which is on top of the drain. Improved memory density comes from the ability to stack one transistor on top of another, fully using the third dimension for the first time. The implications for lithography are profound. The most critical dimensions, like the gate length, are no longer lithographically defined but rather are determined by film thicknesses. In fact, the lithography requirements are significantly relaxed: the first release of 3D flash chips is likely to require only 50-nm lithographic features (single patterning!). Lithography will be relaxed, but the etch requirements will be extremely challenging. The burden of transistor density improvements will no longer be upon lithography.

I believe that flash will lead the way for other semiconductor devices. Pitch division multiple patterning will allow logic to improve transistor density, especially with regularized designs (approaching the maximum density possible—the cross-bar structure). The idea of “random” logic is disappearing—in the future, all transistors will be on a grid. Eventually, transistors will go vertical in logic circuits, with finFETs as a first step. The gate-all-around transistor (also called the nanowire transistor) will look a lot like vertical NAND flash, and will enable 3D integration. Coupled with 3D chip stacking using through-silicon vias (TSVs), the future of chip integration is up.

What does this mean for lithography? For about 40 years, progress along the Moore’s law trend has been gated by lithography: How small can we make our features while still lowering the cost of making each feature? I see the future as subtly but importantly different. Lithography will always be critical, but other process steps, especially etch, will become increasingly important. Device changes and new materials have become ever more central to each new technology node. Lithography will not be top dog forever.

One thing, however, will remain constant. JM^3 will be the place to publish groundbreaking results in semiconductor nanofabrication. Besides advances in lithography, look in these pages for increased focus on etch as well. Metrology is no longer just about measuring feature size and overlay, but also about enabling new materials and processes, such as finFETs and TSVs. And the application of lithography, etch and metrology techniques to MEMS and MOEMS fabrication will continue to deliver innovative results and devices. As always, the future will be different from the past; now maybe more so.

Chris Mack
Editor-in-Chief