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Control of Integrated Circuit Patterning Variance, Part 2: Image Placement, Device Overlay, and Critical Dimension

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The second of two planned special sections on Control of IC Patterning Variance has been completed. Here are my impressions of this technology field and of some of the papers featured.

Control of device patterns' widths, separations, extensions, and overlaps[1,2] may be broken into two parts: one dealing with variations in one-layer design rules (DRs) and the other in two-layer DRs. These are the topics covered in Part 1 (Metrology, Process Monitoring, and Control of Critical Dimension, which appeared in JM3 Vol. 14, Issue 2) and Part 2 (Image Placement, Device Overlay and Critical Dimension, in this current issue), respectively. Together, they cover almost every aspect of device pattern variation. But, as this guest editor discovered firsthand, a special section "is like a box of chocolates... ."

The field of CD-related metrology for process control, squarely within the scope of Part 1, went through big changes, from CD-SEM–based measurement of critical dimension (CD) to optical scatterometry–based metrology of CD, height, and sidewall angle. The long anticipated applications for direct estimation, monitoring, and control of key process parameters, such as on-wafer monitors of effective exposure dose and focus in lithography, have emerged and enabled tighter control of lithography processes and of patterned device dimensions required for extending optical microlithography. What used to be "off roadmap metrology" is now a part of ITRS, yet only a few glimpses of this can be found in Part 1: Metrology, Process Monitoring and Control of Critical Dimension. Perhaps, it is because the main "movers and shakers" in this field have moved on to other fields or out of the industry. Perhaps, with arguments for direct metrology and control of dose and focus for better CD control settled—despite the issues with tool matching, *in situ* versus standalone, metrology on generic versus dedicated monitor structures, and the lack of standard methods and calibration—this became a routine and often proprietary matter.

However, Part 1 contains discussions of e-beam based metrology and inspection for OPC design and one-layer DR validation—an area where the industry lacks the essential capability to ascertain DR compliance in-line, preferably well before the end-of-line testing. Technical analysis[3] of metrology of edge placement error[4] (EPE) reads like a thriller. It also shows that, even with pattern placement as a floating variable and despite using the same tool and edge detection algorithm, a mere comparison of conventional CD-based versus contour-based metrology is not an easy task. Our industry will, likely, keep demanding such capabilities and debating their accuracy for some time yet.

Dealing with two-layer DRs on real wafers is much more difficult. For example, edge-to-edge overlay[5] (EE OL) in two layers' patterns' separation and extension (also known by application-specific terms "poly-to-active endcap," "contact-to-metal enclosure," "contact-to-metal space," etc.) involves critical dimensions in both patterns and their centerline layer-to-layer overlay. Capability of direct in-line EE OL metrology still does not exist—another gap in DR validation. Although EE OL may be estimated using in-line measurements of two layers' CDs and OL, in IC manufacturing practice,[6] the required CDs and OL are not measured on the same tools or on the same patterns, and their respective control loops are separate. However, two-layer DRs being yield-limiting parameters and OL their largest component, EE OL recently got much attention, with EPE declared as the overlay-related lithography technology showstopper. . . What does EPE, the foundation of model-based OPC, have to do with overlay? Nothing: *this* EPE is not *that* EPE. Although the recent appearance of the term EPE in the industry's dialog on EE OL may appear as a sign of discovery, no new control parameter was identified. It is still the old one, just a new name. The new language denies the very existence of two-layer DRs and ignores the long-present gaps in DR validation and control. Not only is the new language not helpful in closing the technology gaps, the resulting confusion disrupts the industry dialog on the real issues. Be that as it may, confusing language is not an obstacle for you to comprehend Part 2: Image Placement, Device Overlay, and Critical Dimension. Our authors made an effort to "speak standard SEMI" and to use standard JM^3 acronyms whenever possible, and to define or at least illustrate exactly what they mean by the terms which others may find confusing. In one case, you are given the motivation for a new definition, terminology, and performance metric in a new application. Authors rigorously define the subject, explain why those changes are needed, and even trace their new definition to the long-existing SEMI standard. Would you, JM^3 reader, expect anything less?

Control of IC Patterning Variance Part 2: Image Placement, Device Overlay, and Critical Dimension does not have papers on the usual "flavors" of metrology of image placement such as alignment, registration, and overlay. However, there are abundant accounts of metrology of image placement by metrology users, very interesting in their own right: registration metrology on photomasks, modeled and experimental CD-SEM based metrologies of device and alignment/metrology targets' overlay, even of pattern placement in directed self-assembly.

There is also the latest learning of pattern placement variation and of its control: wafer stress-induced component of overlay, charging-induced pattern placement error in photomasks, feature- and tool-specific placement errors in lithography for both device and OL measurement structures, etc.

Part 2 represents a significant advancement in our collective understanding of the sources of IC pattern variation affecting the two-layer design rules, and of the new approaches to their control. Whether you are interested in industry, technology, or competitive learning, Part 2 does not disappoint. Within its broad scope, it contains something for almost every interest and taste. I hope that you will enjoy it, too.

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