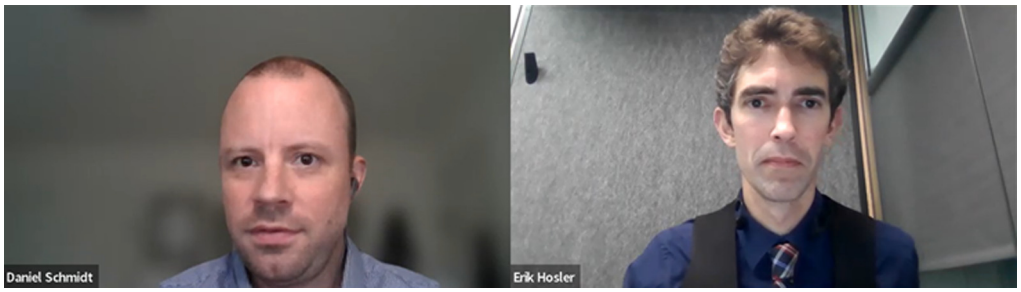
Advances in inline Raman spectroscopy: an interview with Daniel Schmidt



JM^3 Associate Editor Erik Hosler of PysQuantum LLC interviewed Daniel Schmidt of the IBM Thomas J. Watson Research Center about his recent work with in-line Raman spectroscopy. Readers are also invited to enjoy the interview in video format, https://bcove.video/3eABypl.

JM^3 Associate Editor Erik Hosler of PysQuantum LLC interviewed Daniel Schmidt of the IBM Thomas J. Watson Research Center, one of the authors of "In-line Raman spectroscopy for gate-all-around nanosheet device manufacturing," published in the April-June 2022 issue of the journal.

Erik Hosler: Thank you very much for joining us today. My name is Erik Hosler. I'm a technologist at PsiQuantum, and lithographer by trade. Today, I'm talking with Daniel Schmidt, who is a researcher at IBM, focusing on next-generation technology techniques. And I'm going to be talking to him a little bit about his most recent presentation at SPIE Advanced Lithography, as well as publication in JM3. It's great to be talking with you again today, Daniel.
Daniel Schmidt: Yeah. Hey. Thanks, Erik, for this opportunity to present my work. I'm glad to be talking with you today.

EH: Can you tell me a little about the paper that you've presented?
DS: Sure, thing. Yeah, absolutely. So the paper is really dealing about inline Raman spectroscopy for nanosheet devices. We purchased, essentially, a Raman tool, and wanted to convince, first and foremost, ourselves that the tool that we've purchased is working the way it's supposed to do. The primary goal here was to evaluate the capabilities of the inline tool with regards to nanosheet materials characterization. So we really wanted to focus primarily on channel strain, because that's really a big research topic when we're talking about nanosheet transistor architecture. Specifically for the PFET transistor, you're actually taking a performance hit with the nanosheet transistor because of the electron mobility, or the hole mobility specifically for the PFETs. So, strain is really a big topic there, and you want to be able to measure and monitor this, ideally non-destructively, inline, in the manufacturing line.

So all of the research efforts and the initial TCAD modeling, simulation, verification experimentally; there was a lot of research effort ongoing. And essentially, everything was verified by destructive metrology. Of course, in manufacturing, or even earlier, in development, you cannot just keep cutting your devices to verify what's the strain, because then you don't have any electrical data anymore afterwards. In optical metrology, Raman specifically, really is the materials characterization technique here that we were interested in using to characterize strain, because Raman is a well-established lab technique that has been proven over decades for strain metrology.

We wanted to show that this is possible inline, that we can keep, or that it can monitor our devices, specifically the channel strain in the manufacturing line. So that was really the key of the paper. We went in and ran, essentially, a few different test wafers through the entire front-end-of-line processing, starting all the way at the very beginning when we deposit the alternating nanosheets stack, comprising silicon and silicon germanium multi-layers, epitaxial layers. The silicon layers will eventually form the channels of the transistor. And then we took that all the way through the front-end processing and kept measuring with our Raman tool at the various steps. Essentially, every patterning step, after every critical patterning step in the route, we used our Raman tool, measured the data and analyzed the data, and tried to compare that wherever possible to non-destructive other reference techniques, predominantly that was XRD at the blanket, unpatterned stage, as well as after fin patterning, we took X-ray diffraction reference data. It was quite challenging actually to analyze these, inline specifically, after the patterning. And then also, later in the stage, we did destructive TEM techniques, transmission electron microscopy. There are techniques available, specifically nanobeam diffraction or precession electron diffraction, with which you can determine the strain.

We compared that reference metrology to our inline data, and we found that these are matching very well. So we've essentially shown in the paper that we can track the strain evolution in the nanosheets from the blanket stage all the way up to channel release. That's when you have the freestanding silicon channels, just before you do the high-k metal deposition. And we can use Raman metrology for that strain characterization. So that's really what the paper is all about, to prove to ourselves first and foremost, and then through the publication, by extent to the industry, that, yes, inline Raman is a capable technique to monitor strain in the channel.

EH: And how did you find a strain involved with the nanosheet processing?
DS: It has actually quite an interesting development throughout the processing. So first up, the only thing that's really strained at the blanket stage is the silicon germanium layers, and the silicon sheets are strain free. And then as soon as you start your first patterning step, which is essentially comparable to your fin patterning, the germanium layers are starting to relax laterally, and that induces the first strain in the silicon channel.

And then through your subsequent processing: STI, start with your dummy gate, you do your SiGe indentation. The strain is actually successively increasing, more or less, on a high level, successively increasing.

And then once you do your silicon germanium release so that you have your freestanding silicon channels, that's the step when you actually have a significant relaxation again, because now there's no pinning anymore. The silicon germanium is not there, that introduced that strain into the silicon channels. So you have a significant relaxation at this point. And that really depends now on the device dimensions, essentially. The lateral dimensions are defined on how much relaxation the device is experiencing.

That was actually, also, one of the nice results of the paper. We had a different sheet, or sheet width and sheet length, and we could nicely see that the dimension has a critical impact on the relaxation. And really, a nice result was that this also matched of course the simulations that were done independently of that study and published prior to our experimental verification.

EH: OK, excellent. And how does Raman scatterometry compare to more typical inline scatterometry techniques?
DS: That's a good question. That's very interesting. You're talking about Raman scattering, and you're talking about scatterometry. So both have the word scatter in there, and it seems to be something to do with scattering. But apart from the fact that they're both optical non-destructive techniques, they're basically looking at completely different things. So when we do Raman spectroscopy, we look at Raman scattering, and that means we look at inelastically scattered light. We're typically shining a monochromatic laser on a sample, and we try to—we are evaluating the light that comes back that is different in energy. It can either gain or lose. Typically, at room temperature, you're losing the energy.

So we're looking at Stokes Raman scattering, so that the energy that's coming back from the sample is slightly lower than the incident laser beam. And this energy loss that's roughly happening in the frequencies of the infrared range, we detect that with a visible detector. And that's

essentially a fingerprint of the material under investigation. Based on the energy loss of that initial frequency, you can determine composition of the material, you can determine strain—that's what we did predominantly for our study in the paper—but you can also look at crystallinity, for example.

So, Raman is really a materials characterization technique. Whereas, scatterometry, it's really looking at elastically scattered light. So here, we are looking only at—typically, you're shining broadband light at an angle, at an angle of incidence onto the sample, and you measure the polarization state change of that reflected light.

Essentially, the sample can be considered a mirror. So you shine light at a specific angle onto the sample, and we analyze the reflected light that is elastically scattered. Here, we were only looking at a polarization state change. That means an intensity ratio and a phase change of that light.

So now, with scatterometry specifically, you need rather complex analysis models. You need to build a three-dimensional unit cell, and then it goes through RCWA calculation. So, rigorous coupled wave analysis. And then you basically solve the inverse problem. You do a minimization algorithm with your floating parameters. And at the end of the day, if you did everything right, you would get dimensional parameters. That's predominantly used for a dimensional analysis.

And that's not to say that you can't also do materials characterization with scatterometry, but the typical use case is really, scatterometry is dimensional metrology, Raman metrology is really a materials characterization technique.

So I would say, these are the two buckets that you can put them in on a high level. Sure, you can use one for the other. But again, that's how I would place them.

EH: In the context of doing metrology on stacked nanosheets, the ability to have material-specific information is extremely valuable, I could see.
DS: Yes.

EH: In the paper, you talked about this in terms of a vertical traveling scatterometry technique. So can you talk a little bit more about how that works?
DS: Yes. This is our most recent paper that we have published just this year that is really decoupled from the Raman study. So we have just this year introduced with our partner Nova, a technique called vertical traveling scatterometry. And that's a completely new and novel technique that's, I would say, very disruptive to the industry because it brings an entirely new aspect to scatterometry. What it does is it makes use of what's called spectral interferometry, and that gives you access to the absolute phase of the light. So with a lot of math and some tricks, you can actually convert now your measured spectrum into depth information. And then you can apply filters, and basically filter your scatterometry information based on the depth on where it's coming from. So, why this is really, really interesting is that you can now go in and measure fully integrated devices without actually having to model the full stack. We had shown a few different examples. And going back to the nanosheet, where this ties a little bit back to the Raman. We did measure M1—so, the first metallization level—on top of a fully integrated nanosheet device, that had the nanosheets, it had the gate stack, full gate metallization, and then we were interested in monitoring the M1 on top of that fully integrated nanosheet transistor. And the reason this is important because, the more we start scaling, the more these minute differences between the metrology targets in the scribe line and what's going on in the device area, these minute differences start to become not so minute anymore, and you really want to actually measure where it matters.

So with that vertical traveling scatterometry, VTS for short, you can measure on fully integrated devices. By now applying that filter, we basically can just cut off all of that spectral information that is coming from the nanosheet transistor underneath. And so we can focus on the first metallization, on the optical information that's coming from that first metallization layer, and therefore have a much, much easier optical model built. So our optical model is actually really the lines and spaces of the M1 layer, and we don't need to care about the information that's coming from the nanosheet stack underneath.

So that's really a big disruptive step forward in being able to use scatterometry on fully integrated devices.

EH: Yeah, absolutely. Speaking back to your previous point about setting up the models and all of the math involved. The more you can simplify those models and that math, the easier all of our lives will be in the industry.
DS: Yeah. And specifically mine. Specifically mine.

EH: Yeah, exactly.
[LAUGHING]

EH: So you've talked about two new emerging techniques for metrology that you've applied to gate-all-around devices. What's your outlook on how these techniques will play out in the industry for both leading edge CMOS, as well as the beyond-Moore type devices, particularly considering 3D devices that you've talked about here?
DS: Right. So I honestly believe both of these techniques are here to stay. Raman spectroscopy, there was an attempt to introduce this to the industry, probably about a decade ago. And that was probably too early. There was more of a research type need at that point. Now that we really are going into third dimension, starting with, essentially, FinFET. Now the nanosheet architecture is so intricate. And if we're looking further down the scaling roadmap with stacked FETs, and scaling further down, Raman specifically is a critical technique. Because, due to the laser that's being used, you can really go very small spot, and you can do very fast measurements. Depending on the sample that you're looking at, you can do really fast measurements with Raman technique.

If you do have a couple of different wavelengths available, you can vary, by correct choice of wavelength, your penetration depth on where the information is coming from. If you use a UV laser, for example, or a very short wavelength laser, you get information only from the top of the sample. If you use a longer wavelength laser, you penetrate deeper into the sample. So you get that depth information through choice of wavelength.

Now, scaling further, what's also critical to notice is that the higher the aspect ratio, the more unlike the material properties are in that canyon. For example, let's make an easy example: source/drain area.

The higher the aspect ratio of that source/drain area where you need to deposit your source/drain material, the less comparable it becomes to what you do on a blanket. So, traditionally, you would monitor your deposition and your material properties on a blanket. You would probably use ellipsometry or XPS, for example, to characterize that particular deposition.

Now, if we scale further, the canyons become smaller and smaller, the aspect ratio, higher and higher. Now your material does not behave exactly anymore as it does on the open area. Meaning, your deposition does not behave any more exactly the same as it does in the open area.

So you really need to measure on patterned targets to understand what you've just deposited. If you want to deposit a silicon germanium in your source/drain area, with a certain germanium content, you've got to measure on a patterned target to understand what's exactly the germanium concentration.

Raman is one of the key techniques going forward to help us understand that. We can probe with a short wavelength, essentially, the top of that source/drain epi. With a longer one, we can go all the way through that source/drain epi. We have a lot of degrees of freedom characterizing, for example, that source/drain material.

So again, in my opinion, Raman going forward is here to stay. It's going to help us in manufacturing for nanosheet devices, and it's going to help the development for the stacked transistors, if we put N and PFET on top of each other. Scatterometry, specifically the VTS as an additional tool in our metrology toolbox, is possibly very important for the stacked FETs. If we want to measure something that's happening, or the processes that are designed to happen only for the top transistor, we don't really want to model that entire three-dimensional transistor.

Let's say, if N is at the bottom—one polarity is at bottom, the other one is at the top. Traditional scatterometry, you would have to model the entire stack, which requires a lot of floating parameters, and it's just a modeling nightmare really. It requires a lot of engineering time to do that.

Vertical traveling scatterometry can really help us significantly here, by just setting a filter, a depth dependent filter to cut off anything that's coming from a deeper region, and we can focus, for example, only on the top part of the transistor during the manufacturing cycle.

So again, both of these techniques that we've introduced in the past two years, I think are going to be very, very valuable for many, many years to come.

EH: What do you see the impact outside of more traditional CMOS applications?
DS: That's a good question. So, I mean, for Raman specifically—well, I should say for both of these techniques really. If you think about—one example would be neuromorphic computing. So you need to introduce memory devices in the early back end. One key word would be a memristor for neuromorphic compute.

So you need to introduce that memory device in the early back end. And that brings a lot of metrology challenges. I mean, apart from, obviously, a lot of processing challenges, it brings a lot of metrology challenges with it. So we have, all of a sudden, a tiny device in otherwise a metallized back end. We do have new materials, completely new materials for these memory devices that we have not seen in the line previously for traditional CMOS. So here, Raman, and also specifically VTS, the vertical traveling scatterometry, can help tremendously. Raman for the characterization of the materials that go in. They are usually very complex multi-component materials. That's the secret sauce that goes into all of these devices. That needs to be controlled. The manufacturing of or the deposition of these materials needs to be controlled very, very carefully because they directly impact the performance of the devices.

You want to have a good materials characterization technique to monitor the stoichiometry, for example. And you want to be able to have a good dimensional characterization technique, like VTS. So you can measure these memory devices on—or these memory features that are on top of an otherwise fully integrated CMOS circuit.

But you don't want to model that. You want to characterize how thick is my film. What's the dimension after etch? And potentially any other materials metrology, dimensional metrology that you can think of that's required for that memory device. But you don't want to model the entire stack. And here, again, VTS is an absolute key technique and makes our life much easier.

So, outside of traditional CMOS, that neuromorphic computing is really one area where both of these techniques can help. And for Raman in general, anywhere where you have materials characterization needs. Think of LEDs, III-V semiconductors, gallium arsenide, whatnot. Silicon carbide, for example, it has a lot of different phases. Raman is the technique that can help you to characterize them.

And then at the horizon of the roadmap—I mean, fine, that goes back to CMOS, but not necessarily. We have all these two-dimensional materials that are coming our way. We've seen already a few publications really coming from the industry, where graphene, for example, was used. Historically, if you look at Raman papers, for any two-dimensional materials paper that's out there, there is at least one Raman metrology being done on it.

And I think that's also where Raman metrology really gained its broad popularity, really, I think. Once graphene was discovered, everyone needed to do Raman metrology to characterize the D and G peaks to be able to say, this is how many layers of graphene I have, and this is the crystal quality. If my defect peak's not there, I have perfectly single crystalline graphene. And that needed to be done with Raman.

And these materials are making their way into manufacturing at some point. So, Raman is really the key characterization technique here that we have at hand to characterize these. Together with some others, like AFM, XPS, for example. We have already quite a toolbox available for what's coming up, but we're not stopping.

EH: You'll always need a fully stocked toolbox on these emerging technologies, but I agree with you. I think both the vertical travelling scatterometry, as well as the Raman-based technique that you've explored here on gate-all-around devices, really does represent a needle mover for metrology for some of these emerging devices, particularly for magnetic tunnel junctions. It's a complicated stack there. And being able to do metrology on that stack *in situ*, non-destructively, that could potentially be a game changer as this technology evolves.
DS: Yes. Yeah, I agree.
EH: So with all these great things, what's the next big thing that you see yourself working on?
[LAUGHS]

DS: That's a question where I have to be careful on how I answer that. We do have a really excellent partner ecosystem in Albany, and we have access to a lot of tools in the alpha, beta stage. So it really feels like we do work on the next big thing all the time. That's really what the job here, makes it really exciting. So one thing I can say, IBM has just recently published a little bit of a roadmap on where we're heading in terms of semiconductors. And to no surprise, we put out a strategic goal on demonstrating a stacked FET transistor in 2024. So if you want one answer to that question, the next big thing is probably showing metrology on a stacked FET transistor.

EH: Awesome. You do bring up a good point about the Albany ecosystem. Here, your papers are run in collaboration with vendors, but also within IBM. Looking down the road, do you see this as being the standing paradigm for metrology development and proof points will be done? Will it be done primarily through collaboration, or are we moving more towards the phase of manufacturers developing their own differentiated metrology techniques to gain an edge?
DS: Yeah. I mean, I think the model that we have here, the collaborative approach going forward is really synergistically very valuable for both parties. I mean, the manufacturing or R&D side really has that key insight on what's needed next. We know what we're working on, so we know what upcoming metrology challenges there are, and what the needs are to really drive the development. I mean, historically, most of the tools that we have available today are either developments that came from university research institutes or manufacturing companies. If you take IBM, for example. AFM. Scanning probe microscopy AFM. Showing atomic resolution with AFM. That's coming from IBM.

And now we have several vendors that are selling inline tools, and there's a lot of development ongoing to really make AFM an inline capable technique. We need to increase speed so that it really becomes viable, we need to probably work on the tips so that there's not that much wear per scan, and so on and so forth. So we do see a lot of developments historically coming out from the manufacturer. And also, recently, if I look at some of the SPIE presentations, there are very interesting developments coming out of Samsung, for example, where they look at sphere-assisted optical metrology going below the diffraction limit.

So this is really exploratory research that's ongoing. But in my opinion, ultimately, it takes a vendor to take this from the lab to the fab. You've got to have that full engineering stack to make all these improvements and these tweaks, such that that technique ultimately is ready for inline use. So, at the end of the day, this collaborative approach is really the most beneficial in my opinion.

EH: I think it's always better to work as a team. I think that's a good point, Daniel. So, I think, with that, we'll wrap things up. Thank you very much for talking with me today, Daniel, about your most recent papers and the great work that you guys are doing over at IBM.
DS: Yeah. It was a pleasure to talk to you. Thank you very much, Erik.