

Review of scanning electron microscope-based overlay measurement beyond 3-nm node device

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Abstract. Overlay control has been one of the most critical issues for manufacturing of leading edge semiconductor devices. Introduction of the double patterning process requires stringent overlay control. Conventional optical overlay (Opt-OL) metrology has technical challenges with measurement robustness, solving overlay discrepancy between overlay mark and device pattern, and measuring smaller marks laid out in large numbers within the die accurately for high-order correction. In contrast, scanning electron microscope-based overlay (SEM-OL) metrology can directly measure both overlay targets and actual devices or device-like structures on processed wafers with high spatial resolution. It can be used for reference metrology and optimization of Opt-OL measurement conditions. SEM-OL uses small structures, including actual device patterns, which allows insertion of many SEM-OL targets across a die. Precise overlay distribution can be measured using dedicated SEM-OL mark, improving measurement accuracy and repeatability. To extend SEM-OL capability, we have been developing SEM-OL techniques that can measure not only surface patterns by critical dimension SEM but also buried patterns for leading edge device processes. There are two techniques to detect buried patterns. One is to use high-acceleration voltage SEM, which detects backscattering electron emphasizing material contrast. It has been adopted for overlay measurements for memory and logic devices at after-etch inspection or even after-develop inspection. The other is to utilize charging effect, which reflects voltage contrast at the surface depending on the material properties of underneath structure. SEM-OL measurement using transient voltage contrast has been developed and its capability of overlay measurement has been proven. An overlay measurement algorithm using template matching method has been developed and was applied to dynamic random access memory (DRAM) process monitor in manufacturing. In order to extend SEM-OL metrology to beyond 3-nm node logic and cutting-edge DRAM devices (half pitch = 14 nm), we are improving measurement precision of detecting buried patterns and measurement throughput by developing optimized SEM-OL mark. © 2019 Society of Photo-Optical Instrumentation Engineers (SPIE) [DOI: [10.1117/1.JMM.18.2.021206](https://doi.org/10.1117/1.JMM.18.2.021206)]

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1 Introduction

Optical overlay (Opt-OL) instruments are most commonly used for overlay metrology in semiconductor manufacturing. Two Opt-OL metrology techniques, image-based overlay (IBO) and diffraction-based overlay (DBO) are applied in advanced semiconductor manufacturing. IBO instrument is bright field microscopy, which uses the standard method of optical microscopy systems. Dedicated targets for IBO, like box in box, have been adopted as the IC manufacturing overlay standard target for years.¹ In 2003, advanced imaging metrology (AIM) mark was optimized using overlay mark fidelity (OMF) as metrics.^{2,3} OMF is an estimate of overlay measurement variability due to process robustness of the overlay target and the overlay metrology process. AIM mark consists of grating targets that are patterned on the reference and current layer. Both target types are mirror symmetric with 0 baseline (same centerline). AIM mark has longer pattern edge than in SEMI Standard box in box targets,¹ and it also uses edge-based symmetry detection for the grating targets. Periodic patterns are useful for many methodologies.

On the other hand, DBO instrument measures diffraction efficiencies of the diffracted orders from specially designed stacked gratings that are set as overlay targets.⁴ The measured data are a function of the overlay. Diffraction from the overlay target is simulated with rigorous coupled wave approach,⁵ and it depends on the optics and sample condition. It requires time for optimization of the target and recipe creation.⁶ One of the standard dedicated targets for DBO metrology is μ DBO target.⁷ μ DBO target translates a lateral position difference between two layer gratings in a stack into an asymmetry in the angle-resolved diffraction. The relative merits of optical IBO and DBO in manufacturing environment are still being debated especially considering robustness and accuracy issues on wafers with target asymmetry and variations. Process- and target-specific wavelength optimization, measurement quality metrics, and calibration to scanning electron microscope-based overlay (SEM-OL) measurements are being pursued.^{8–10}

Tool-induced shift (TIS) is evaluated to estimate the impact of tool asymmetry on measurement error.¹¹ TIS can be obtained by measuring overlay at 0 deg and 180 deg of wafer rotation and the difference of the two divided by 2. Once an estimate of TIS is available, this error can be removed from OL measurement, improving overlay metrology accuracy and tool-to-tool matching. TIS evaluation, optimization, and calibration have been automated on all

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commercial Opt-OL tools. Testing for TIS is also useful in alignment applications.¹² Pattern size of the Opt-OL target is typically from 100 to 1000 nm, and target size is typically from $7 \times 7 \mu\text{m}$ through $30 \times 30 \mu\text{m}$.¹³ Opt-OL metrology has a technical challenge in measuring smaller marks placed in large numbers within field and segmented pattern in the mark.¹⁴ Conventional Opt-OL metrology uses a dedicated target with larger size and different structures than device patterns. The Opt-OL measurement results at after-develop inspection (ADI) were shifted due to scanner lens aberration depending on the pattern sizes of optical metrology targets, which are significantly larger than device patterns.^{15–19} Wafer-induced shift (WIS) is introduced to account for the errors due to pattern asymmetry of the overlay targets.²⁰ It is induced by process steps such as etch²¹ or chemical-mechanical polishing (CMP).^{22–24} Asymmetric etch causes shift of where the pattern centerline is at its top versus its bottom and the target asymmetry, leading to error of conventional OL metrology. CMP causes an asymmetric profile at the top of the target, leading to asymmetric optical image, and OL measurement error. Nonzero overlay correction in lithography, taking into account pre- and postprocessing, was evaluated to improve final pattern and yield.²¹

SEM such as critical dimension SEM (CD-SEM) is generally used for measurement of CD in semiconductor production. SEM-OL metrology had been discussed for decades.^{25–28} It can directly detect edges of device pattern or device like pattern with high spatial resolution and measure overlay using the edge positions. SEM-OL metrology is completely different from Opt-OL metrology interaction with the sample and measurement error mechanisms. It is an image-based technique and therefore has many things in common with the optical IBO metrology. In many critical applications cases, where optical OL metrology may suffer from processing related signal variability and measurement inaccuracy. SEM-OL metrology can be used for reference metrology and optimization of Opt-OL measurement conditions.

Since around 2008 when double patterning technique was introduced to enable further pattern size shrinkage, overlay control has been one of the most critical issues for semiconductor device manufacturing. To improve residual error after correction, higher-order correction to compensate the nonlinear overlay errors, correction per exposure (CPE) to correct overlay errors in each individual field have been applied in addition to linear correction to correct the intrafield and interfield overlay errors.^{29,30} For the overlay corrections, small OL mark has been needed to be laid out in large numbers within die.

The requirements for overlay measurements became rapidly stringent; measurement discrepancy between Opt-OL mark and device pattern became a serious issue to be managed in semiconductor processes. To solve this issue, Hitachi High-Technologies began developing SEM-OL techniques to measure actual device patterns directly or device-like target at after-etch inspection (AEI).^{31,32} For initial optimization of Opt-OL metrology, SEM-OL metrology has been used as a reference.³³

In around 2012, the demand of layer-to-layer overlay measurements between surface patterns in device area at AEI using SEM-OL has increased.^{34,35} To detect reference patterns partially covered by the current layer pattern, overlay measurement algorithm, inspection and process qualifier

(iPQ), was developed for process monitor in manufacturing.³⁶

Since 2014, we have studied the SEM-OL in collaboration with imec. We designed and evaluated dedicated targets for SEM-OL metrology. With arrival of three-dimensional structure devices and shrinking of device size, the overlay measurement between surface pattern and buried pattern by insulator film, namely see-through-overlay measurement, became indispensable in manufacturing of memory devices, especially DRAM. Then high-voltage SEM was developed to fulfill these requirements.^{37,38} SEM-OL measurements made it possible to feedback to mask or scanner linear overlay 10 correctable terms. It was applied for improvement in R&D, Technology Ramp and for process monitor in manufacturing.^{39,40} We will review SEM-OL metrology applied in current CD-SEM and high-voltage SEM (HV-SEM).

For logic devices (and not only memory devices), see-through-overlay measurement enables high-order overlay correction with scanner because SEM-OL can measure the small dedicated target within $2 \times 2 \mu\text{m}$, which is easy to be laid out in large numbers within a die. For beyond 3-nm node and cutting-edge DRAM device process, it is required to control the overlay within 2.8 nm ⁴¹ and to measure the precision within 0.3 nm . HV-SEM and small measurement target have been used for high-order overlay correction.

As outlined above, over the years, conventional Opt-OL metrology has been putting much effort into both basic technology development and specific applications learning, managing to improve its accuracy and repeatability as required. As the result, Opt-OL continued to be viable as primary overlay metrology in production. Although SEM-OL metrology showed a great deal of promise, recently becoming the main supplemental technology and the reference metrology for Opt-OL, especially when it comes to measurement accuracy in the presence of target asymmetry and manufacturing process variations, better representing device overlay, up to now it did not become the main process monitor. In this paper, we will review and illustrate significant recent advancement in SEM-OL metrology technology and in SEM-OL applications for advanced nodes. We will also consider one additional barrier to technology entry, the slower throughput of SEM-OL metrology tools.

2 Dedicated Mark and Algorithm of SEM-OL metrology

Figure 1 shows a schematic diagram of SEM contrast. Topography and material contrast are the most typical contrasts in conventional CD-SEM or HV-SEM. SEM at low accelerating voltage ($<2 \text{ kV}$) measures the secondary electron (SE) image. SE emission especially increases on specimen tilt area like pattern edge. Contrast provides information of the surface topography. When reference pattern at ADI is covered by blanket film, it is not detected by low-energy electron beam. CD-SEM is used for overlay measurement at AEI in this paper. SEM-OL metrology by CD-SEM will be discussed in Secs. 3–5. HV-SEM measures the SE image and/or back scattering electron (BSE) image. Contrast mainly provides information of surface profile and surface or buried composition by material contrast. It can be used for overlay measurement at ADI and AEI. SEM-OL metrology by HV-SEM will be discussed in Sec. 6.1.

	Topography contrast	Material contrast	Voltage contrast (VC)	
			Steady charging state	Transient charging state
Model				
Factor	Edge	Atomic mass	Resistance	Capacitance

Fig. 1 Typical SEM contrasts and their physical mechanisms for overlay measurement. Schematic explaining mechanisms and the factors are shown.

On the other hand, voltage contrast is caused by charging under electron beam irradiation. At steady state, image contrast depends on the difference in resistance of specimen, because the emitted SEs result from the stable currents flowing into the resistor.²⁸ At transient state, emitted SE is affected by the accumulation of charge. So transient voltage contrast depends on capacitance between the surface and the substrate including buried structures.^{42,43} Buried pattern detection by transient voltage contrast will be discussed in Sec. 6.2.

For SEM-OL, in collaboration with imec, imec N10 back end of line (BEOL) short loop to create metal 1 (M1) and via 0 (V0) logic and static random access memory (SRAM) devices was used. The M1 patterns are split into three images placed in three different plates (M1A, M1B, and M1C) and V0 patterns are split into two images placed in two different plates (V0A and V0B). The exposures are performed on NXT1950i scanner from ASML. The lithography process is using a negative tone development resist. We will review the evaluation results in Secs. 3, 4, and 6.

Figure 2(a) shows an example of the dedicated SEM-OL target between the metal layer and via layer for overlay X.

Current pattern is 96-nm pitch and 24-nm trench patterned M1A exposure. Reference pattern is 24 × 32 nm hole patterned by V0A. Scan direction of SEM is normally left to right with respect to wafer notch. Pattern layout between the current and reference layer is like a part of AIM mark for optical IBO. The current patterns are dense trenches (grating) in the metal layer and reference patterns are dense holes in via layer, respectively. It was selected to prevent current and reference patterns from overlapping when large overlay error occurs for the evaluation. Each layer pattern is of the same size as dense pattern under the layout rule. The dedicated target for overlay Y, which rotates counterclockwise 90 deg with respect to the target for overlay X, is located in the vicinity of the target for overlay X. Scan direction of SEM for overlay Y is normally top to bottom with respect to wafer notch. Overlay Y is measured by the same procedure for overlay X in consideration of image rotation. Although, additional dedicated marks for overlays X and Y, which rotates counterclockwise 180 deg and 270 deg, respectively, should be laid out for mark symmetry⁴⁴ like AIM, they were not evaluated at this time. Alternatively, interlace pattern as a dedicated SEM-OL mark between M1A and M1B, which

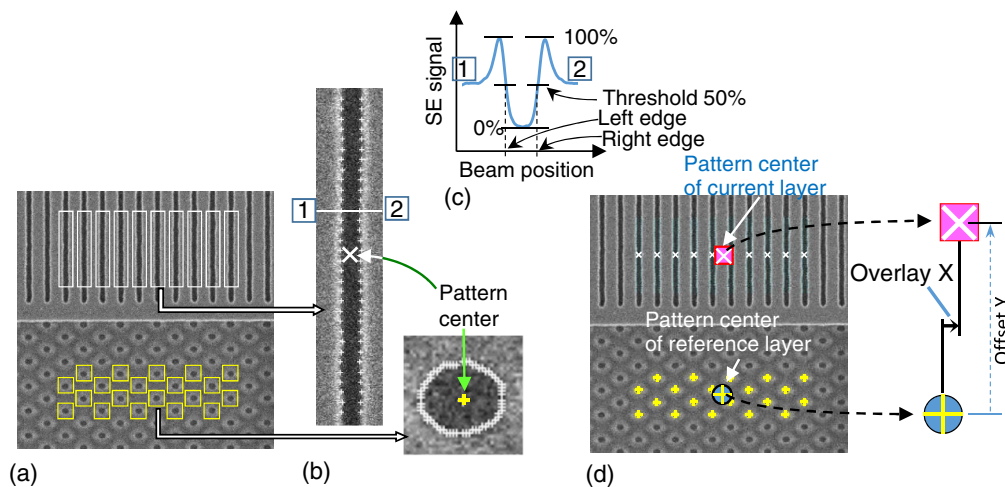


Fig. 2 Example of dedicated SEM-OL mark for explanation of the measurement algorithm for overlay X (a) dedicated OL target for SEM-OL metrology whose reference and current layer is V0A and M1A, respectively in this example, (b) detected pattern edges of trench and hole pattern, and the pattern center calculated as the mean of pattern edge coordinates, (c) pattern edge method with threshold of 50%, and (d) pattern center of reference and current patterns calculated as the mean of each pattern center coordinate. Enlarged view of two pattern centers shows calculation method of overlay X.

has pattern symmetry, was evaluated in Sec. 4. Also line and space patterns by single exposure were laid out for evaluating influence of pattern size and image rotation.

Figure 2 shows SEM-OL measurement algorithm. An example of a dedicated target for overlay X measurement is shown in Fig. 2(a). Scan direction of SEM for overlay X is left-to-right with respect to wafer notch. The pattern edge is detected for each pattern using conventional threshold method.⁴⁴ It is found with the cursor box [white and yellow boxes to check the pattern area in Fig. 2(a)]. In the automatic measuring system, the position of the cursor box is decided by template matching with the registered image.

Figure 2(b) shows each pattern edge and the pattern center. Right and left edges of the trench are detected 36 points, respectively. Edges of the hole are detected at 48 points. Pattern center is calculated as the mean of edge coordinates. The threshold for edge detection is set to 50% [Fig. 2(c)]. Pattern centers for current and reference layers are calculated as the average of all the patterns position coordinates for each layer [Fig. 2(d)]. Then the overlay vector is determined as the difference of coordinates of pattern centers for each layer [Fig. 2(e)]. For this case, overlay X is x component of the overlay vector, which is as-designed zero offset in horizontal direction. Offset Y in Fig. 2(e) is not used for overlay measurement. For overlay Y , which rotates counter-clockwise 90 deg with respect to the target for overlay X , the target is located in vicinity of the target for overlay X .

TIS in SEM-OL measurements had been evaluated.^{25,45} Rosenfield et al. have optimized the SEM accelerating voltage, detector design, and scanning technique to reduce TIS. In this paper, three factors are mainly considered to improve TIS in SEM-OL. First is charging caused by the interaction of the electrons with the specimen. Asymmetry of the signal profile is increased in some cases, and it causes a shift of overlay measurement value. It depends on specimen structure and accelerating voltage of electron beam and scan conditions, direction, and scan speed. To reduce the asymmetry, a method using multidirection scans for imaging has been evaluated in Sec. 5.1. When left-to-right scan causes asymmetry between left and right signal profile at pattern edge, measurement using additional right-to-left scan can be applied. At ADI, resist shrink is caused by electron beam irradiation. Normally, resist is shrunk symmetrical in imaging when the resist pattern layout is symmetrical. Therefore, influence of resist shrink to overlay accuracy should be negligible.

Second is SEM image distortion, rotation, and magnification. It influences measured pattern edge distribution. It mainly depends on electron-scanning uniformity in speed within the scan line and on relative displacement of the scan line by magnetic and electric noise. Measurement method and correction method of image distortion have been evaluated.^{46,47} Dedicated SEM-OL mark in Fig. 2 is for overlay X measurement. As for the layout, there is a designed offset Y between pattern centers of the reference and current layer, which is about 800 nm. Image rotation should affect overlay X as measurement error. Image rotation of SEM tool is calibrated. Overlay shift caused by image rotation cannot be measured by method using measurements at 0 deg and 180 deg of wafer rotation. The measurement error will be discussed in Sec. 3. If offset Y in Fig. 2(e) was measured, Y magnification error in SEM image would be unacceptable.

When layout of overlay mark is symmetric and concentric, like in SEMI Standard marks,¹ measurement error due to image rotation and magnification error should be negligible.

Third is tilt of primary electron beam axis. The TIS by the tilt is proportional to the tangent of the tilt angle and difference in height between the reference and current layer theoretically. Tilt is calibrated precisely using inverted pyramid Si substrate, which is obtained via anisotropic etching of crystalline silicon.⁴⁸

Although SEM-OL metrology can measure device pattern directly, measurement of dedicated SEM-OL mark should be selected in some cases. Current pattern edge on device pattern layout is close to the reference pattern edge as via in the trench in the dual damascene (DD) process. Then the edges overlap with each other and degrade the OL measurement accuracy, especially linearity when overlay error is large. Hotta et al.³¹ had developed SEM-OL metrology for double patterning of complex 2-D holes as well as dense lines.

Again, high-voltage electron beam may have potential to damage device property. In that case, a dedicated mark is laid out at a distance from the device area. When a large number for measurements in the field is needed for high-order correction and device patterns within the measurement point is not proper for SEM-OL, dedicated mark is needed around the measurement points. In collaboration with imec, dedicated mark was designed for 10-nm node BEOL process. It is important for design of dedicated SEM-OL mark to be symmetric with zero baseline like SEMI Standard¹ Opt-OL mark, Box in Box, AIM mark, and μ DBO target to keep high measurement accuracy.

Developed techniques and applications for reducing TIS and the optimized SEM-OL target are effective in improving the repeatability of SEM-OL measurement.

Current move-acquire-measure (MAM) time of SEM-OL measurement by CD-SEM is below 2 s. To ensure high precision, MAM time of HV-SEM is currently about 10 s for low S/N signal BSE images evaluated in Sec. 6.1. In order to extend SEM-OL technique to beyond 3-nm node logic, improved measurement precision of detecting buried patterns and higher measurement throughput are required for more stringent overlay control. Measurement throughput is being improved through an image processing technique for low S/N images and application for sequence before image acquisition.

CD-SEM images were acquired using Hitachi CG5000, operated at low accelerating voltage of 800 V. At the low voltage, collected signal is mainly SE. CD-SEM on this condition cannot detect buried pattern, which includes reference pattern at ADI. This condition is selected for higher yield of SE and needed for high-resolution measurement. CD-SEM can detect pattern edge for SEM-OL measurement at AEI. In some case, to detect edge signal of current and reference patterns simultaneously or edge signal of the trench or hole bottom, higher accelerating voltage from 1 to 5 kV is applied. It will be discussed in Sec. 5.

3 Evaluation of SEM-OL Metrology Using Pattern by Single Exposure

We evaluated the SEM-OL target patterned by single exposure (M1A).³⁹ The overlay between grating patterns with design rule pitch and relaxed pitch was measured at AEI using CD-SEM. In Fig. 3, the details of SEM-OL modules

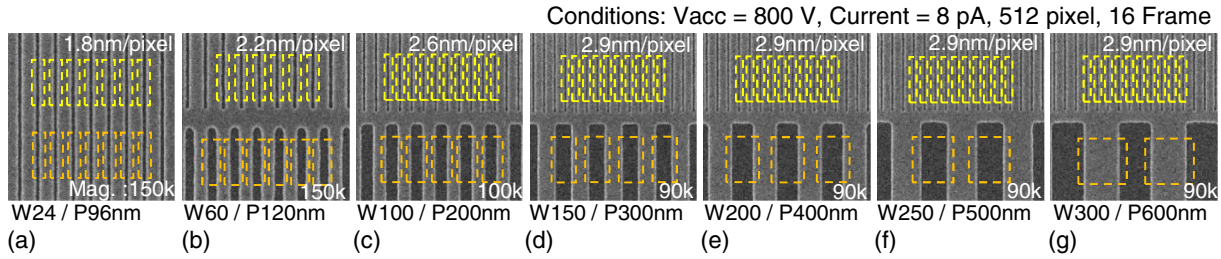


Fig. 3 Images of SEM-OL module using HV-SEM. All patterns are patterned by single exposure. Overlay was evaluated using upper and lower grating in each image, which was defined as current and reference pattern, respectively. Size of current grating in each image is 24-nm width and 96-nm pitch. Width and pitch of reference grating are described under each image. They increase from (a) to (g).

designed for the evaluation are shown. Upper and lower half patterns of each image are defined as the reference and current layer, respectively, in this section. Dimensions of reference and current grating in a group of targets are different. Pattern size of reference grating in each target is a design rule of M1A in common (width = 24 nm and pitch = 96 nm). Pattern size of the current grating in each target is from the device pitch 96 to 600 nm. Grating pitch of optical AIM mark and μ DBO target is typically from 200 to 2000 nm.⁷ Every target in Fig. 3 is for overlay X measurement and as-designed zero offset between the reference and current pattern in horizontal direction. Scan direction of SEM for overlay X is left-to-right with respect to wafer notch. The dedicated target for overlay Y, which rotates counterclockwise 90 deg with respect to the target for overlay X, is located in the vicinity. Scan direction of SEM for overlay Y is top to bottom with respect to wafer notch. The sampling plan was two targets at each site for both overlays X and Y, 6 sites in a chip, and 9 chips in a wafer (54 measurement points in total).

The target for 24-nm current patterns in Fig. 3(a) consists of long-trench patterns through the top and bottom of the FOV (without line tip). Averages of 54 measurements of both overlays X and Y are not zero but 0.03 and -0.07 nm, respectively. One of the reasons for nonzero value is image rotation. It is very small because it is calibrated in advance. In this paper, TIS was measured without image rotation factor.

Figure 4 shows repeatability, which is 3σ of measurements repeated 10 times with wafer load and unload. Repeatability of overlays X and Y for 24-nm current patterns in Fig. 3(a) is 0.14 and 0.17 nm. Repeatability of image rotation will be estimated based on symmetry pattern results in Sec. 3. The repeatability of the target including wider current pattern is degraded from 0.2 to 0.3 nm because total line

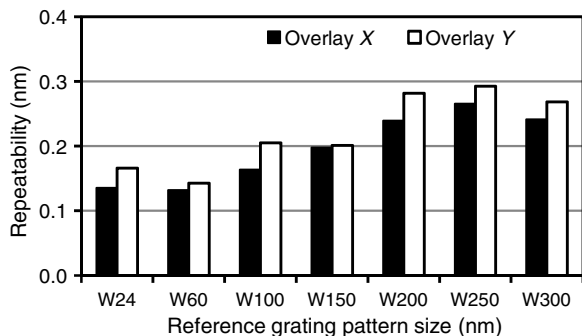


Fig. 4 Repeatability of SEM-OL measurement for the target shown in Fig. 3. Repeatability is defined as 3σ of 10 repeated measurements.

length in the current layer for measurement is shorter and pixel size is about 3 nm at magnification 90k and 512 pixel imaging. Measurement results of each site in field are average of measurement in nine chips (points). Therefore, repeatability of averaged result is estimated to be about 0.1 nm ($=0.3/\sqrt{9}$). TIS of overlay X for reference grating pattern size: 24,100 and 250 nm is -0.01, 0.12, and 0.16 nm, respectively.

Overlay shift within intrafield on six locations through the field is measured as shown in Fig. 5. Six measurement areas are located on upper left (UL) and right corner (UR), and lower left (LL) and right corner (LR), and upper center (UC) and lower center (LC) end in the field. The graph shows the overlay between grating in design rule pitch (96 nm) and grating in various pitches. In the X coordinate, W_{xxx} indicates the line width of current grating. The field is 26×16 mm. To evaluate overlay variation in the field with respect to each target, averaged overlay of 54 measurements is subtracted from measured overlay at each point. Every point is the average of nine fields over the wafer. Shape in the graph shows horizontal position in the field (circles are on the rightmost, squares are on the leftmost, and triangles are on the center).

The results show that larger grating size gives larger overlay range in the intrafield fingerprint (the maximum range is

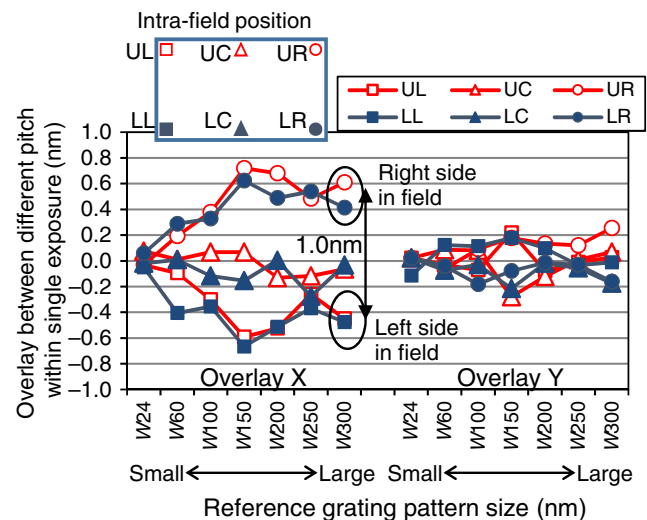


Fig. 5 Overlay between device pitch and other pitches, which are patterned by single exposure. Intrafield positions, UL, UR, LL, and LR correspond to upper left and right corner and lower left and right corner in field, respectively. UC and LC correspond to upper and lower center end in field.

1.0 nm on overlay X). The effect seems to be mainly a slit size and pitch issue. This is widely known to be related to coma aberration fingerprint of the i -ArF scanner^{16,17} but has not been simulated. Overlay error was caused by scanner aberration depending on a variability from tools and the illumination condition of the scanner, which is decided from the typical pattern feature. Therefore, in-die overlay using larger size pattern has potential for having discrepancy from the actual device pattern. Overlay measurement using device pattern size is effective to reduce the discrepancy.

4 SEM-OL for Dedicated Mark using CD-SEM

In Fig. 6, the details of CD-SEM overlay modules are shown. There are three types of targets. The first and second modules are designed for overlay measurement in the multiple patterning layer (M1B to M1A and V0B to V0A, respectively) after hard mask (HM) etch. Dimensions patterned are the same in both layers. Third module is designed for overlay measurement in layer-to-layer in DD process (M1A to V0A) at AEI. In the imec N10 process, metal-first and self-align process were applied. Therefore, large trench in the metal layer should be patterned over via area to detect via pattern edges precisely in AEI. The trench size should be optimized to prevent WIS for overlay in manufacturing, because etching conditions on large trench area may be not the same as in the device area, and via pattern in the mark have potential to be degraded in edge contrast. Dedicated SEM-OL mark can be designed within $2 \times 2 \mu\text{m}$, the size easily allows its placement in many locations for in-die overlay. Every target in Fig. 6 is for overlay X measurement and as-designed zero offset between reference and current pattern in horizontal direction. The dedicated target for overlay Y , which rotates counterclockwise 90 deg with respect to the target for overlay X , is located in vicinity. Scan direction of SEM is the same as evaluation in Sec. 2. The sampling plan was two targets at each site for both overlays X and Y , 1 site in a chip, and 10 chips in a wafer (20 measurement points in total).

The repeatability, average of TIS and TIS variation over the wafer for the three evaluations are presented in Table 1. Repeatability and TIS variation are 3σ of measurements repeated 10 times with wafer load and unload. Overlay mark between M1B and M1A is interlace pattern with symmetry. Measurement points for each layer are selected so that the pattern centers of M1A and M1B are as-designed zero offset. The results are sufficient for overlay metrology for 3-nm node. The repeatability, 0.11 nm, is improved from that of

Table 1 SEM-OL performance in multiple patterning layers (M1B to M1A and V0B to V0A) and in layer-to-layer in DD process (V0A to M1A) at AEI.

Current to reference		Repeat.	TIS	
		3σ (nm)	Ave. (nm)	3σ (nm)
M1B to M1A	OL X	0.11	-0.01	0.10
	OL Y	0.11	-0.01	0.07
V0B to V0A	OL X	0.14	0.13	0.17
	OL Y	0.17	0.11	0.18
M1A to V0A	OL X	0.25	0.01	0.29
	OL Y	0.30	0.05	0.28

measurement in Fig. 3(a) with asymmetry condition, 0.14 and 0.17 nm. It is caused by variation of image rotation and less total measured line length on the measurement in Fig. 3(a).

Results of overlay for V0B to V0A and M1A to V0A at AEI are not sufficient for overlay metrology for 3-nm node. Especially, repeatability of overlay for M1A to V0A is degraded by low contrast on V0A hole pattern edge in Fig. 3(c). The edge seems to be rounded off at M1A HM etching. It will be improved by optimizing scan conditions (scan speed and accelerating voltage, etc.), using well-designed dedicated mark. Repeatability for overlay measurement is improved by higher resolution imaging (smaller pixel size or larger frame number) and by increasing the number of measurement points (edge length).^{49,50} The relationship between repeatability and throughput should be taken into account when SEM-OL is considered as an alternative for Opt-OL measurements.

Figure 7 shows CD-SEM imaging for SRAM pattern after DD etching.³⁷ This layout has via-in-trench with large metal trench region. CD-SEM can measure overlay in SRAM region between V0 and M1 directly. The repeatability of overlays X and Y is 0.31 and 0.47 nm, respectively. They are larger than the dedicated target because it depends on number of via and trench length.³⁰

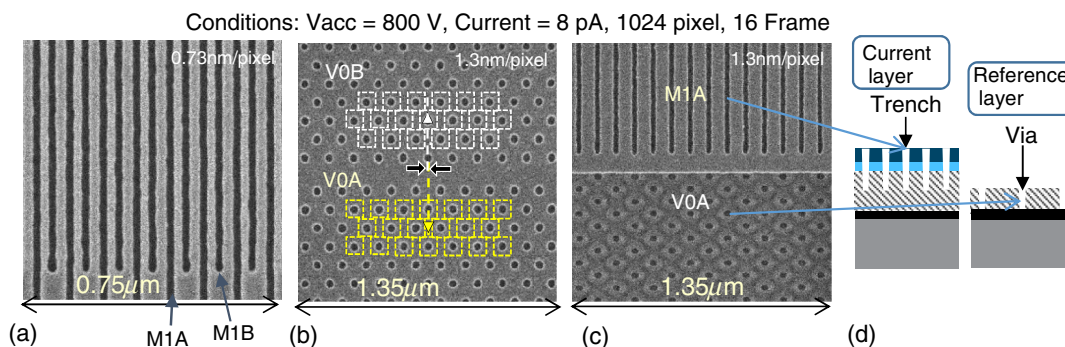


Fig. 6 Images of SEM-OL module using CD-SEM at AEI: (a) M1B to M1A after M1 HM etch, (b) V0B to V0A after V0B HM etch, (c) M1A to V0A after DD etch, and (d) schematic cross section for overlay for M1A to V0A.

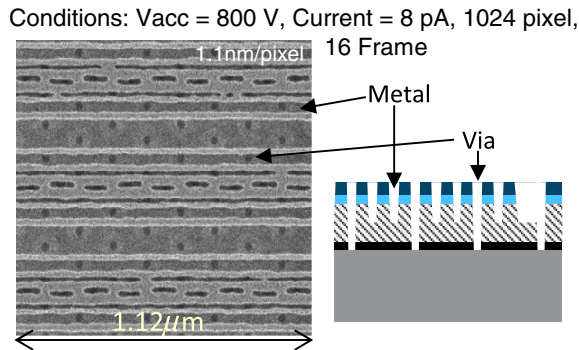


Fig. 7 CD-SEM imaging for SRAM pattern after DD metal etching and the schematic cross section.

Results of the correlation of SEM-OL at AEI and optical IBO are shown in Fig. 8. IBO measurements are performed using Archer 200 tool from KLA-Tencor with standard AIM marks. The sampling plan was two targets at each site for both overlays X and Y , 1 site in a chip, and 150 chips in interfield. We checked the linearity with Opt-OL using a program-shifted wafer. In the correlation, both the slope and R -square are close to 1, indicating good correlation shown in Table 2. Offset of overlay between M1B and M1A is within 0.17 nm with symmetry of SEM-OL mark. On the other hand, offset of overlay between V0B and V0A and between M1A and V0A is larger. It was caused by asymmetry of SEM-OL mark and overlay discrepancy between the hole of SEM-OL mark, which is the same size as the device, and large width line of Opt-OL mark. Net residual error (NRE) is defined as $3\sigma/\sqrt{2}$ of difference between two techniques. NREs are within 2.1 nm for overlays X and Y , which include measurement uncertainty and CD-SEM overlay, precision of Opt-OL, sample variations of both optical and SEM targets, and overlay variation due to distance of the Opt-OL and SEM-OL marks. The distance is from 200 to 700 μ m. Hotta et al.³² have evaluated NRE between overlays at two sites as a function of the distance, which begins to increase at about 1000 μ m. It should be considered for the evaluation. Measurement uncertainty of CD-SEM overlay will be improved by optimized mark design regarding symmetry pattern and increasing edge length.

We have compared values of correction parameter between SEM-OL and Opt-OL in linear 10 correctable terms

Table 2 Correlation between SEM-OL and optical IBO at AEI. Linear regression (slope, offset, and R^2) and NRE which defined as $3/\sqrt{2}$ of difference between two techniques.

Current to reference		Slope	Offset (nm)	R^2	NRE (nm)
M1B to M1A	X	0.97	-0.17	0.95	1.0
	Y	1.03	0.16	0.95	1.0
V0B to V0A	X	0.99	0.55	0.97	2.1
	Y	0.98	-0.77	0.97	2.1
M1A to V0A	X	1.02	0.35	0.98	1.6
	Y	1.00	-0.80	0.98	1.6

for intralayer (V0B to V0A) and interlayer (M1A to V0A).^{39,40} The differences are not significant. Six parameters of CPE were compared between SEM-OL and optical IBO. The sampling plan and SEM-OL and optical IBO conditions are the same as correlation of evaluation in Fig. 7.

In Fig. 9(a), six parameters of CPE are extracted for SEM-OL and optical IBO between V0B to V0A after HM etching. Translations X and Y at overlay between V0B to V0A have some programmed trends in the vertical direction by a scanner offset. The distributions show the same tendency. The difference of each 3σ in interfield between SEM-OL and optical IBO is small, although each NRE is large (2.1 nm) in Table 2. In Fig. 9(b), the six parameters of CPE are extracted for SEM-OL and optical IBO between M1A to V0A after DD etching. Distributions of translations X and Y for SEM-OL and optical IBO are similar to each other. The 3σ s of optical IBO is larger than SEM-OL. Four parameters (asymmetry magnification, asymmetry rotation, symmetry magnification, and symmetry rotation) are similar to each other, respectively. However, there are several large differences (>0.08 nm/mm) in CPE parameter between SEM-OL and optical IBO on some shots of wafer center or wafer edge. The maximum difference in the field is estimated about 1 nm because the field size is 26×16 mm and the 3σ s of optical IBO is larger than SEM-OL by

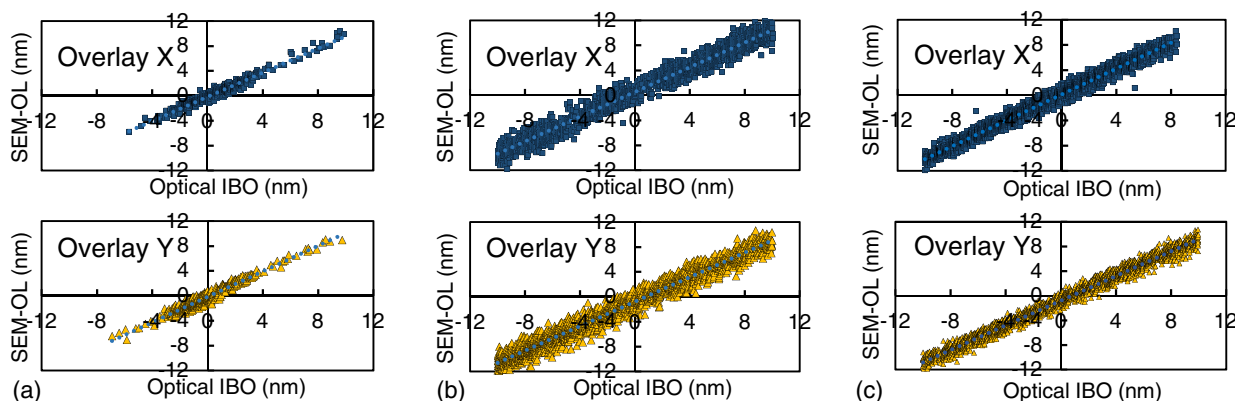
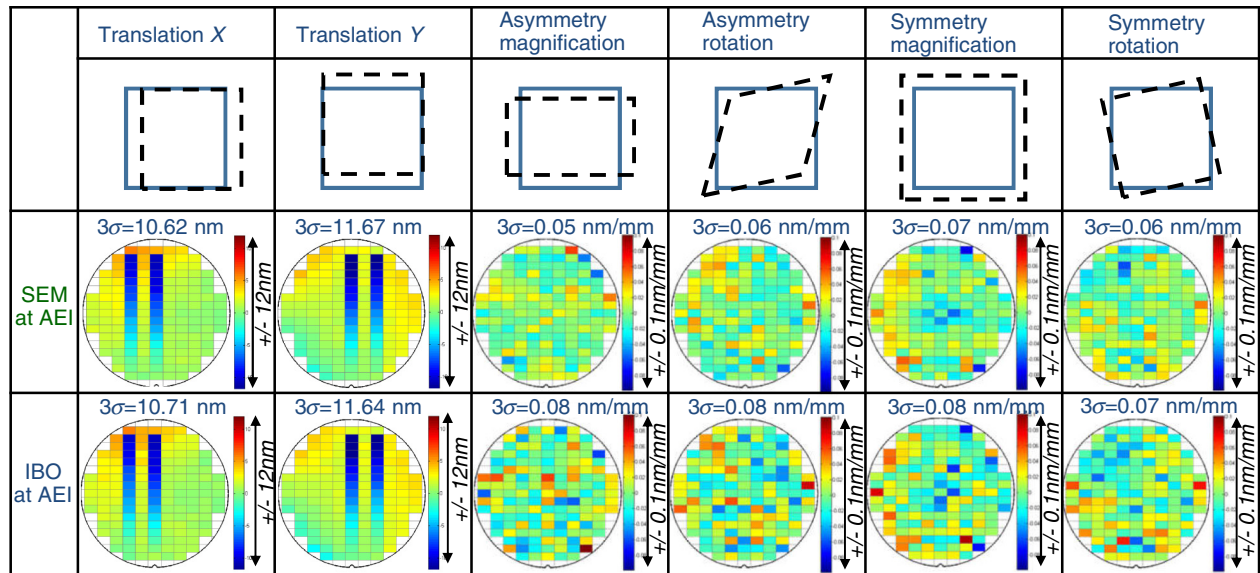
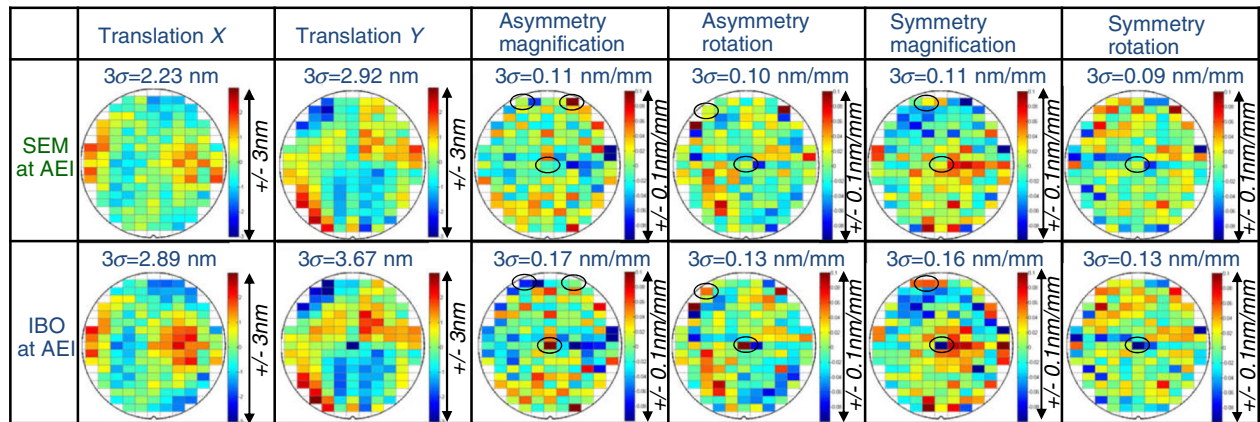


Fig. 8 Correlation between SEM-OL and optical IBO at AEI: (a) M1B to M1A, (b) V0B to V0A, and (c) M1A to V0A.



(a)



(b)

○ : Large difference of CPE correctable between SEM and IBO (>0.08nm/mm)

Fig. 9 Wafer maps of six parameters for CPE which are extracted for SEM-OL and optical IBO (a) between VOB to V0A after HM etching (b) between M1A and V0A after DD etching.

differences from 0.03 to 0.06 nm/mm. Discrepancy between SEM-OL and optical IBO is larger for overlay between M1A and V0A. The reasons include the difference of measurement patterns (trench and hole) and illumination condition of i-ArF scanner between M1A and V0A.³¹

CPE correction is effective in reducing overlay residual. It is expected to reduce overlay error after the correction when the correction is ideally fed back to the scanner. 3σ of overlay residual is a metric commonly used to evaluate the overlay correction in semiconductor manufacturing. Table 3 shows the 3σ of residuals after CPE correction. Each residual is smaller with SEM-OL. It shows CPE by SEM-OL has the possibility to improve overlay error more than optical IBO. However, throughput of current SEM-OL is slower than Opt-OL. Therefore, hybrid overlay metrology using SEM-OL and Opt-OL may be a candidate for effective overlay monitor. Hotta et al. have evaluated hybrid overlay metrology using optical linear correction (10 terms), which is measured at four corners of chips and SEM-OL high-order correction in the intrafield, which is measured at four chips on double patterning process for dense line patterns.³¹

Table 3 Overlay residual after CPE correction.

Current to reference		3σ of residual after CPE (nm)	
		SEM-OL	Opt-OL IBO
VOB to V0A	X	2.0	2.8
	Y	2.1	2.8
M1A to V0A	X	3.4	3.9
	Y	6.4	6.8

5 Overlay for Actual Device Pattern

5.1 Overlay Using Edge-to-Edge Overlay

Charley et al.⁵¹ have evaluated SEM-OL measurement using actual logic device area directly. Fig. 10(a) shows an example of CD-SEM enables one to measure overlay between SiN

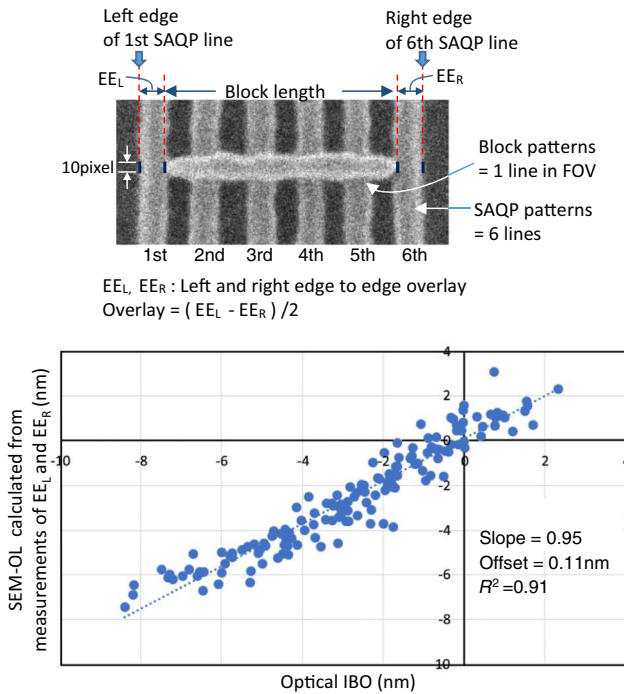


Fig. 10 Overlay between SAQP and EUV block pattern using CD-SEM: (a) SEM imaging and overlay calculation from left and right EE overlays and (b) correlation between calculated SEM-OL and optical IBO.

dense line patterned by self-aligned quadrupole patterning (SAQP) process and SiO block patterned by extreme ultraviolet (EUV) exposure.⁵² Edge-to-edge (EE) overlay⁴ between SAQP line edge and EUV block pattern tip should be controlled.

It mainly depends on line width of SAQP, length of Block pattern, and overlay between SAQP and EUV block. In the case illustrated in Fig. 10, there are six lines patterned by SAQP process. Three parameters (identified: EE_L , EE_R , and the block length) were measured by CD-SEM. EE_L is defined as distance between left edge of first SAQP line and left tip end of block line. EE_R is defined as the distance between the right edge of sixth SAQP line and right tip end of block line. Two line edges and two tips of EE_L and EE_R are detected using averaged SE signal profile for 10 scan lines (of 10 pixel width).⁴⁴

Overlay between SAQP and EUV block is calculated from EE_L and EE_R

$$\text{overlay} = (EE_L - EE_R)/2.$$

Acceleration voltage is optimized to 5 kV to enhance tip contrast of block line pattern on SAQP. To reduce the asymmetry of SEM signal between the left and right tips, a method using multidirection scans for imaging has been applied.

Figure 10(b) shows the correlation plot between SEM-OL and optical IBO. IBO measurements are performed using Archer 200 tool with standard AIM marks. Each data point corresponds to 1 die on the wafer. SEM-OL and IBO data are an average of 10 and 4 points per die, respectively. Over a 10-nm overlay range, the two techniques are correlated ($R^2 = 0.9$) and the offset is small ($=0.1$ nm). This validates the good sensitivity and better representing OL in device

structures of the CD-SEM-based methodology. The factor of discrepancy between the two techniques in Fig. 10(b) may involve fluctuation of the tip edge position of block line pattern, which is not robust to process variation (mask pattern, lithography, and etch). The average of the edge detection is not enough to be used, only averaged measurement results of 10 images using 10 pixels width per image.

5.2 Overlay Using Comparison with Reference Image

For a case where patterns for overlay measurement exist on the surface of an actual device, iPQ using comparison to reference image had been developed.³⁶ The iPQ enables overlay measurements even when the reference pattern edge is partially covered by the current layer pattern or the pattern is too complicated to detect the pattern edge. It expanded the range of application of SEM-OL technique, which has been applied on high throughput review SEM or high-voltage SEM and was used as continuous monitoring of overlay for memory device. The iPQ enables image collection at predetermined points. The proposed overlay measurement algorithm is characterized by comparing test images with a golden image, which has an ideal zero overlay. The golden image is selected by the user from the collected images. Figure 11 shows the process flow of the proposed algorithm. Two pattern regions, first current pattern region (#1 in this figure) and second reference pattern region (#2 in this figure) are recognized from golden and test image automatically by utilizing a “graph cut” technique.^{53,54}

The placement error of the current patterns (dX_c, dY_c) and the placement error of the reference patterns (dX_r, dY_r) are calculated using a template matching method.⁵⁵ Based on the technique, the placement error of the segmented pattern is obtained as a difference between the two images. This developed matching method extracts the position of each pattern contained in two images. Finally, the overlay (e_x, e_y) is calculated from each pattern placement error.

It is not necessary to set up the measurement cursors. This is one of the advantages of the proposed method from a usability point of view. The position of second pattern (layer #2 in Fig. 11) is measured automatically although the edge is partially covered by current pattern. It should be mentioned that the calculated overlay is a relative value based on the golden image.

The basic performance of the proposed method was evaluated with an advanced DRAM device. The target layers, Metal0, and contact are shown in Fig. 12(a). In this experiment, we use a Hitachi High-Technologies Review SEM RS6000 with iPQ for imaging. Overlays between metals in current patterns and contact holes in reference patterns were measured about 2700 points for wafer distribution. Contact hole is partially covered by metal. Figure 12(b) shows a wafer map of the overlay, where the lengths and directions of the vectors correspond to the measurement results. There are differences in the overlay trend at the left side and the right side on the map. It is observed that the boundaries of the shot regions correspond to the discontinuous portion of the overlay direction.

To evaluate the repeatability, overlay was measured 3 times with the wafer loaded and unloaded. The repeatability is defined using deviations of variations among repeated measurements for each site. σ_1 , σ_2 , and σ_3 are the deviations

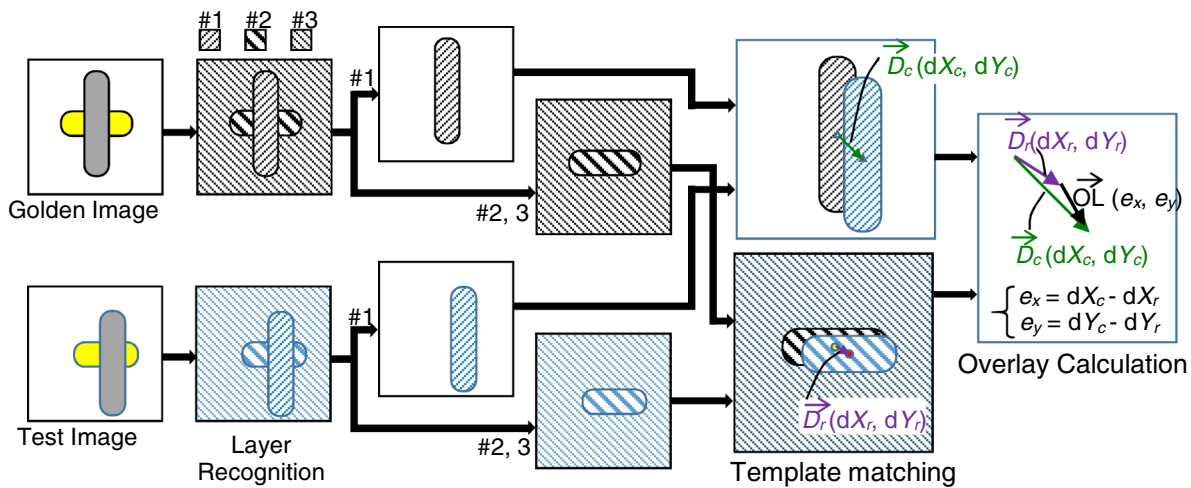
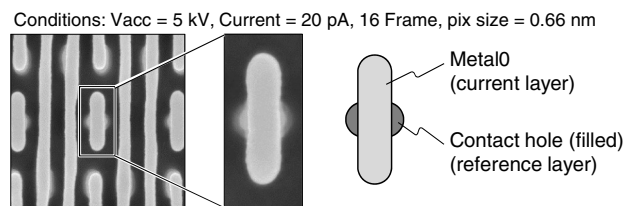
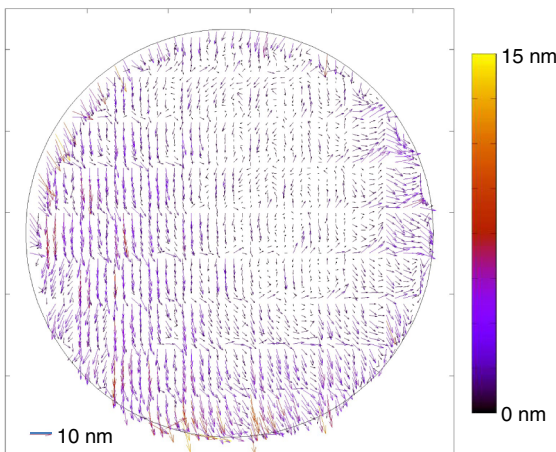


Fig. 11 Process flow diagram of overlay measurement using iPQ. Layers #1 and #2 correspond to the reference layers and layer #3 corresponds to the current layer. A golden image is taken in advance, which has an ideal overlay defined as zero overlay. Overlay of test image is measured using template matching with golden image.



(a)



(b)

Fig. 12 Application result with an advanced memory device: (a) example of image for target layers and (b) wafer map of overlay directions and magnitudes.

of variations between first and second measurement, between second and third measurement, and between third and first measurement, respectively. The repeatability is calculated using root mean squares value of σ_1 , σ_2 , and σ_3 . Repeatability (3σ) of overlays X and Y are 0.85 and 0.92 nm, respectively. A measurement repeatability of 1.0 nm was achieved. Harada has shown the proposed method has linearity and sensitivity for the subpixel order overlay in the numerical experiments even if the patterns have size variations.⁵⁵

6 SEM-OL Metrology for Buried Patterns

6.1 SEM-OL by HV-SEM Using Material Contrast

For a case where reference patterns for overlay measurement exist in the buried layer, SEM-OL metrology technique, which detects buried patterns using BSE or charging-up phenomena as well as measure current patterns using SE, was evaluated. For example, when overlay at ADI is measured, the reference pattern is normally buried by interlayer dielectric film and/or resist. OL measurement results at ADI can be feedback to lithography process immediately. It has the potential to expand the range of application of SEM-OL technique further. Imaging contrast of buried pattern using high-voltage SEM depends on specimen structure and the pattern size. We adopted simulation to evaluate the feasibility and usefulness of an SEM condition.⁵⁶ Characteristic contrasts in high-voltage SEM imaging were well-reproduced in Monte Carlo simulation.

We used HV-SEM, CV5000, to observe the buried pattern using BSE and evaluated the overlay at ADI. The current pattern is resist, whereas the reference pattern is buried pattern. Primary electrons with acceleration voltage of 5 to 30 kV generate SE and BSE when they interact with the specimen. HV-SEM uses two detectors for OL measurement. BSE is captured by the lower detector at the bottom of the object lens and SE is captured by the upper detector. SE generated in the buried layer cannot escape to the surface, therefore, only the surface feature is efficiently observed as SE image. High-energy electrons penetrate resist and capture the difference in the material of the buried pattern. BSE and SE images of the same location can be observed simultaneously. BSE generated on the buried layer penetrates resist again and generates SE with the contrast dependent on the buried pattern. To improve TIS, calibration of the beam axis is performed and is discussed in Sec. 2.

Figure 13 shows SE and BSE images at ADI using HV-SEM. At each optimized condition, SE image shows the resist pattern as the current pattern and BSE image shows the buried pattern as the reference pattern. The edge detection algorithm is the same as SEM-OL using CD-SEM explained

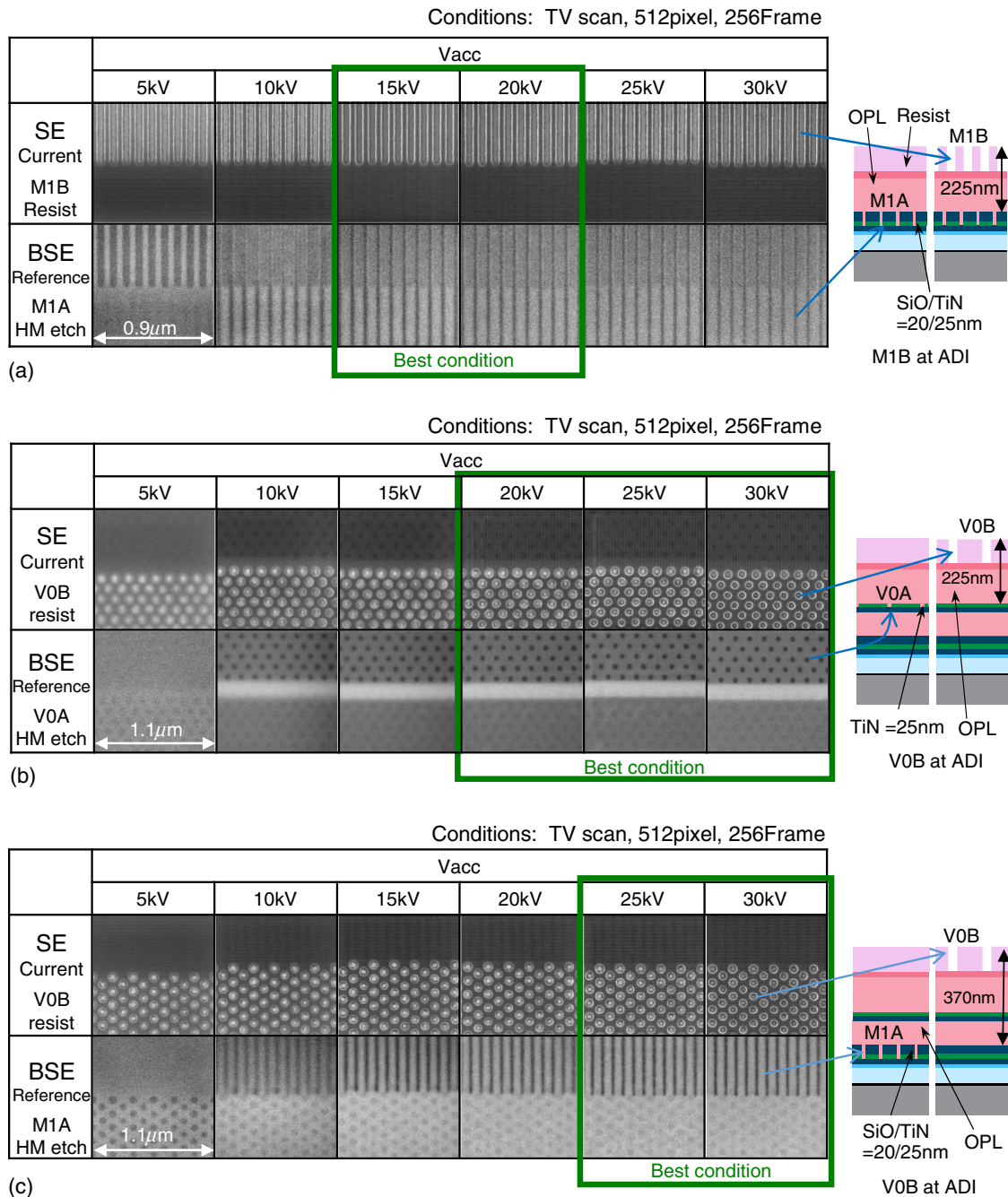


Fig. 13 Images of SEM-OL using HV-SEM at ADI and the schematic cross section. (a) M1B to M1A after M1B lithography, (b) V0B to V0A, and (c) V0B to M1A after V0B lithography.

in Sec. 2. The overlay value is calculated by the difference of the respective points of two images. Figure 13(a) shows acceleration voltage dependence of M1B at ADI. SE image corresponds to M1B resist pattern, and BSE image corresponds to reference M1A pattern in the buried SiO₂/TiN layer. The depth is 225 nm from resist surface to SiO₂/TiN layers whose thicknesses are 20/25 nm. The M1A pattern is not visible at 5 kV but can be seen at 10 kV or higher acceleration voltage. The contrast ratio of line and space of 15 to 20 kV was the best. When the acceleration voltage is 25 kV or higher, the contrast becomes lower since primary electrons transmit through the buried SiO₂/TiN layer. From this result, acceleration voltage of 15 kV was chosen as

evaluation condition. The V0B at ADI needs two types of overlay measurement: overlay for V0B to V0A and for V0B to M1A. Figure 13(b) shows images for overlay for V0B to V0A at ADI. SE image corresponds to V0B resist pattern, and BSE image corresponds to reference V0A pattern in the buried TiN HM layer. The depth is 225 nm from the resist surface to the TiN HM layer whose thickness is 25 nm. When confirming the acceleration voltage dependence, the reference layer pattern is confirmed at 10 kV or more, and the contrast ratio is equivalent at 20 to 30 kV. From this result, acceleration voltage of 25 kV was chosen for evaluation condition. Figure 13(c) shows images for overlay for V0B to M1A at ADI. SE image corresponds

Table 4 SEM-OL performance in multiple patterning layers (M1B to M1A and V0B to V0A) and in layer-to-layer (V0B to M1A) at ADI.

Current to reference		Repeat.	TIS	
		3 σ (nm)	Ave. (nm)	3 σ (nm)
M1B to M1A	OL X	0.47	0.37	0.50
	OL Y	0.45	0.67	0.48
V0B to V0A	OL X	0.25	0.23	0.33
	OL Y	0.23	-1.60	0.74
V0B to M1A	OL X	0.21	-0.57	0.71
	OL Y	0.25	-0.06	0.92

to V0B resist pattern, and BSE image corresponds to reference M1A pattern in the buried SiO₂/TiN layer. The depth is 370 nm from resist surface to the SiO₂/TiN layers whose thicknesses are 20/25 nm. 25 kV or higher acceleration voltage is the optimized condition based on the contrast ratio. The acceleration voltage of 25 kV was chosen for evaluation condition.

Repeatability average of TIS and TIS variation over the wafer for the three evaluations is presented in Table 4. Repeatability of M1B to M1A is >0.4 nm. Some TIS values of overlay for V0B to V0A and M1A are >1.0 nm. This is not enough for overlay metrology for 3-nm node. These parameters are degraded from SEM-OL at AEI in Sec. 4. Degradation of repeatability is mainly caused by charge-up and damage of specimen by irradiation of EB during 10 time measurements. Factors of TIS increasing involve asymmetry of signal profile and difference of specimen damage between 0-deg and 180-deg measurement during evaluation. Reoptimization of SEM condition (acceleration voltage, magnification, scan mode, etc.) and dedicated target design and evaluation method is needed to improve them to meet logic overlay measurement specification. The results depend on specimen condition. In these cases, buried patterns are trench or hole in 25- or 45-nm thickness layer. Material contrast is mainly between the pattern (SiO₂ or TiN) and organic planarization layer.

Results of the correlation of SEM-OL at ADI and Optical DBO are shown in Fig. 14. DBO measurements are performed using Yield Star S-200 from ASML with standard μ DBO target. The sampling plan was two targets at each site for both overlays X and Y, 8 sites in a chip, and 15 chips

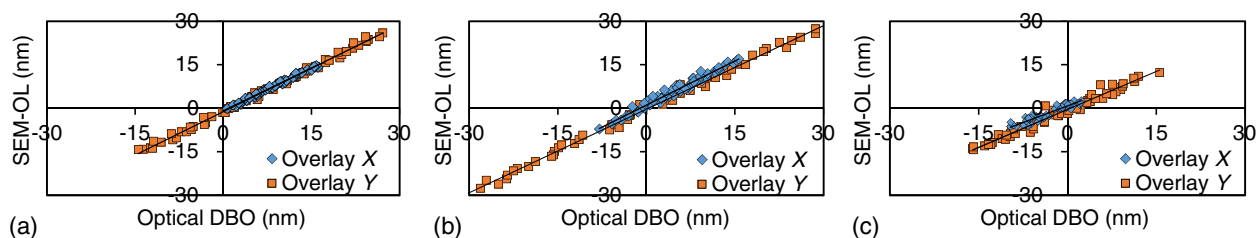
Table 5 Correlation between SEM-OL and Optical DBO at ADI. Linear regression (slope, offset, and R^2) and NRE which defined as $3/\sqrt{2}$ of difference between two techniques.

Current to reference		Slope	Offset (nm)	R^2	NRE (nM)
M1B to M1A	X	0.92	-0.51	0.98	1.4
	Y	0.95	0.22	0.99	1.2
V0B to V0A	X	0.98	-0.79	0.99	1.6
	Y	1.00	1.17	1.00	0.9
V0B to M1A	X	1.02	1.14	0.97	2.0
	Y	0.96	-0.32	1.00	3.1

interfield. We checked the linearity with Optical DBO using a program-shifted wafer. In the correlation, both the slope and R -square are close to 1, indicating good correlation shown in Table 5. On the other hand, some offsets of overlay for V0B to V0A and for V0B to M1A are >1 nm. It may be caused by charge-up and damage of specimen. NREs of overlays X and Y for V0B to M1A are larger than 2 nm, which include factors that are the same as evaluations at AEI in Sec. 4, measurement uncertainty and CD-SEM overlay, precision of Opt-OL, sample variations of both targets, and overlay variation due to distance of the Opt-OL and SEM-OL marks.

6.2 SEM-OL by Low Voltage SEM Using Transit Charging State

HV-SEM using high-irradiation energy for buried pattern detection has potential for a damage of device properties. Therefore, we are evaluating new scan (VT Scan) with low irradiation energy.^{42,57,58} It detects transient voltage contrast for subsurface imaging in Fig. 1. Modulated electron irradiation system enables to optimize condition for signal detection. Figure 15(a) shows a schematic diagram of experimental set up for VT scan evaluation. The system is basically a low-voltage scanning electron microscope. Main feature is pulsating electron irradiation system, which enables accurate control electron dose at pulse width T_p . Pulsating electron beam is generated by a function generator installed with the flood-electron-gun. In addition, imaging system for pulse electron microscopy is developed and transient signals are detected at selected timing and time-width

**Fig. 14** Correlation between SEM-OL and optical DBO at ADI: (a) M1B to M1A, (b) V0B to V0A, and (c) V0B to M1A.

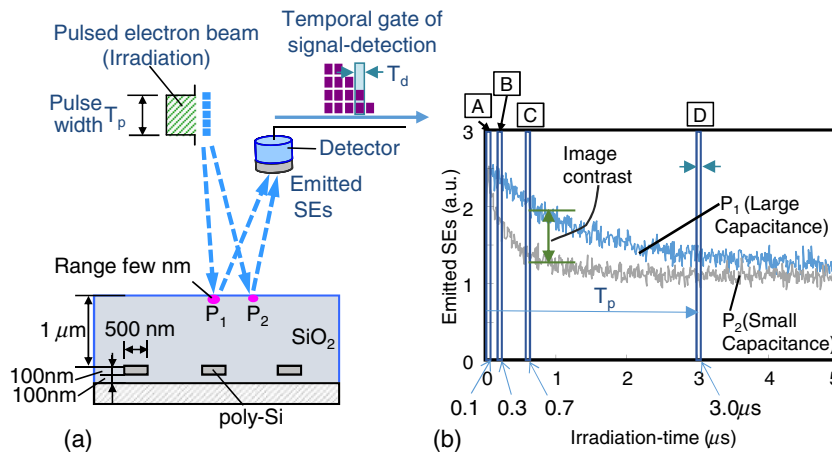


Fig. 15 (a) Schematic diagram for VT scan set up, P1 with underlayer and P2 without underlayer and (b) decay of emitted SE signal at P1 and P2 by continuous irradiation. Difference of decay rate creates contrast between P1 and P2.

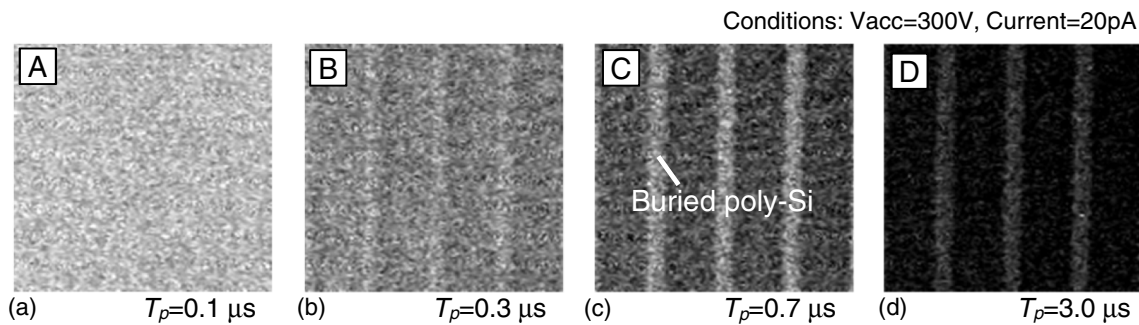


Fig. 16 SEM imaging of VT scan whose contrast between with and without under layer is dependent on pulse time T_p . Each T_p is (a) 0.1 s, (b) 0.4 s, (c) 0.7 s, and (d) 3.0 s.

T_d . Structure of test specimen in Fig. 15(a) is the 1.2- μ m-thick SiO_2 layer, which contains 100-nm thick Poly-Si pattern buried at 1.0- μ m depth. Point 1 (P1) is with buried structure, which is Poly-Si pattern, and Point 2 (P2) is without buried structure. Capacitance of structure under P1 is larger than P2. Energy of primary beam is 300 eV and irradiation current is 20 pA. Under the condition, transit of emitted SEs by continuous irradiation is shown in Fig. 15(b). The emitted SEs decrease with irradiation-time, because part of generated SEs returns to specimen for an increase in positive charge on the surface. The decay rate of emitted SEs at P1 is slower than P2. The difference in the emitted SEs enhance at the transient state until T_p is about 0.7 μ s. This result indicates that the difference in decay rate depends on the difference in the capacitance caused by buried structure.

Figure 16 shows SEM imaging at each T_p condition. At $T_p = 0.7 \mu$ s, buried Poly-Si pattern contrast can be detected most clearly. The most effective condition of T_p for buried pattern contrast depends on the specimen structure and the pattern size.

In Fig. 17, see-through observation using buried Cu specimen is shown using VT scan. Cu, which is covered by SiO/SiOC, was detected at several VT scan conditions. The depth from the surface to the buried Cu layer pattern is 320 nm. Acceleration voltage is low under 500 V. This condition is the same or lower than the standard condition for CD measurement. VT scan at middle T_p in Fig. 17(b) detected buried Cu most effectively. The VT scan enhances the charge

contrast with optimization of T_p . Buried patterns and structures can be visualized using difference of dynamic electrical properties. The VT scan condition is calculated using RC property of device circuit. While VT scan was developed for

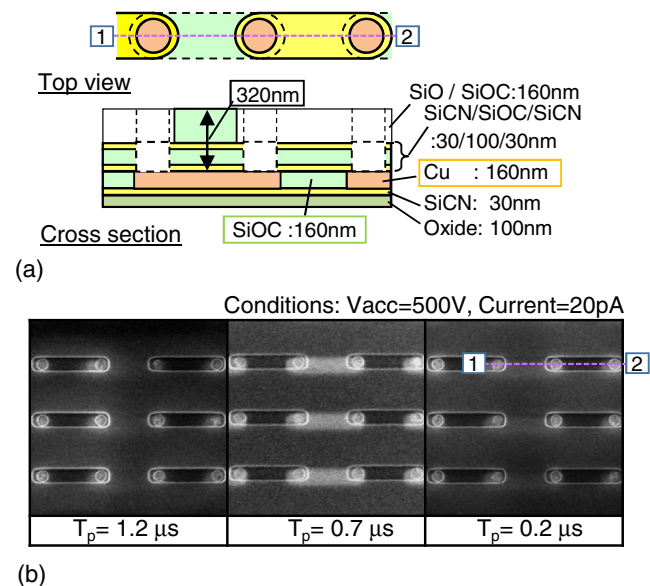


Fig. 17 SEM imaging of device like structure using VT scan: (a) schematic cross section of specimen and (b) SEM imagings that are dependent on condition of T_p .

Hitachi DR-SEM, this technique may be applied to SEM-OL as well.

7 Conclusion

SEM-OL metrology can directly measure device structure and provide overlay information for device patterns. It can be used for reference metrology and optimization of Opt-OL measurement conditions. Accuracy and repeatability of overlay measurement will be improved by optimizing SEM conditions and using well-designed dedicated mark. Conventional edge detection algorithm and method of comparison with reference image have been applied to obtain overlay measurements with good precision in both cases. Tight overlay control also requires overlay distribution correction in a die to higher order than linear components in order to reduce residuals after correction. SEM-OL uses small structures, including actual device patterns, which allows insertion of many SEM-OL targets across a die, and precise overlay distribution can be obtained. On the other hand, large target of Opt-OL metrology has limitation of measuring overlay distribution in a die. Thus SEM-OL metrology might become complementary or alternative technique to conventional optical metrology for overlay control.

To extend SEM-OL capability, we have been evaluating SEM-OL techniques, which can measure not only surface patterns but also buried patterns. There are two techniques to detect buried patterns; one is to use HV-SEM, which detects backscattering electron reflecting material contrast. The other is to utilize charging effect, which reflects voltage contrast at the surface after accumulation of electron depending on the material properties of underneath structure. High-voltage SEM has been adopted to overlay measurement for memory and logic devices at AEI or even after lithography process, which enables immediate feedback to scanner. SEM-OL measurement using transient voltage contrast has been developed and its capability of overlay measurement has been proven without any sample damage as low-acceleration voltage condition was applied.

In order to extend SEM-OL technique to beyond 3-nm node logic and cutting edge DRAM devices, measurement precision of detecting buried patterns and measurement throughput needs to be improved for more stringent overlay control.

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