GUEST EDITORIAL

DOUBLE-PATTERNING LITHOGRAPHY

Shrinking feature sizes through high-resolution optical lithography continues to drive progress in the semiconductor industry by increasing device density while simultaneously reducing fabrication costs per transistor. Continuing the lithographic shrink is the highest priority for many workers in this field. Recently, with the introduction of 1.35-numerical-aperture (NA) ArF immersion scanners, the smooth progress due to numerical aperture increase has come to an end. Water-immersion single-exposure lithography is limited to about 40-nm half pitch with a NA of 1.35. Extension of immersion with high-index fluids and glasses is theoretically possible, but faces severe challenges in technology, economics, and timing. In order to extend water-immersion lithography further, much attention is given to reducing effective k_1 to less than 0.25 using double-patterning lithography (DPL). DPL can take many potential forms including pitch division through successive lithography and etch patterning steps, frequency doubling using spacer or self-aligned processes, as well as innovative processes requiring nonlinear resist exposure. Which forms will be used for device manufacturing will depend on fundamentals such as process capability, yields, cycle time, and overall cost.

This special issue of JM^3 includes ten papers that explore the unique challenges of double patterning for device manufacturing. These papers were originally presented at the 2008 SPIE Symposium on Advanced Lithography. These versions have been peer reviewed, revised, and improved.

The first two papers by Finders et al. and Hazelton et al. establish the budgets for exposure tool critical dimension (CD) control and overlay to meet the needs of double patterning for integrated circuit production. Double patterning creates some new and complex questions about the meaning of feature size control and overlay as features are now created by the edges of successive patterning steps. As a result, CD uniformity (CDU) and overlay become entangled. The paper of Bubke et al. addresses the requirements for the mask. The strict CDU and overlay requirements established in the first two papers mean much tighter mask registration and feature size control is needed for double patterning. Noelscher et al. explores the use of a litho trim to achieve very low k_1 factor spacer double patterning. Spacer double patterning has been widely adopted among memory manufacturers since it can be practiced with existing fab equipment. However, it is a complex and expensive process compared to standard single-expose and etch processes, and it requires an additional mask to remove unwanted stringers formed at some edges. Crouse et al. present data from work to develop lithography-only double-patterning-capable resist processes, which could allow significant cost reduction compared to processes that require spacer formation and removal or intermediate etch steps. Versluijs et al. explore how to pattern 30-nm half-pitch metal layers using a process that stabilizes a first resist pattern by covering it with a polymeric coating, which is then resistant to subsequent etch steps and can be removed by ashing. The paper of Ausschnitt and Halle reports the use of a novel overlay target that enables simultaneous measurement of overlay errors among many mask/layer combinations. Imagine the issues introduced when a mask layer is split in two patterning steps, and then successive critical layers, each likewise split in two, must be overlaid on the first layer! The Blossom target is proposed as an efficient monitor for these combinatorial overlay errors. The paper of Carlson and King Liu explores a negative and iterative spacer process capable of patterning sub-30-nm lines and holes. Not only is spacer double patterning attractive for its ability to create patterns below the Rayleigh limit, but also edge-defined gates have superior CD uniformity and linewidth roughness compared to lithographically defined gates–an important consideration for variability sensitive tools such as static random access memory devices. The paper of Wallow et al. explores the link between shrinkage and 3-D pattern distortions at line-ends and elbow corners where a photoresist has been UV cured to stabilize it in a litho-freeze litho-etch process flow. Finally, the paper of Lee et al. reports the results of modeling the feasibility and performance of nonlinear resist systems for use in double-exposure mode. The development of such materials, if feasible, could dramatically improve the cost of multiple-patterning lithography.

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Guest Editor