REVIEW

# Review of virtual wafer process modeling and metrology for advanced technology development

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**Abstract.** Semiconductor logic and memory technology development continues to push the limits of process complexity and cost, especially as the industry migrates to the 5 nm node and beyond. Optimization of the process flow and ultimately quantifying its physical and electrical properties are critical steps in yielding mature technology. The standard build, test, and wait model of technology development is a major contributor to time and cost overruns. The growing inability to characterize many of the subtle and complicated features and yield limiting factors of a given technology is another serious constraint. We demonstrate the use of process modeling, virtual wafer fabrication, and virtual metrology in process development of advanced logic and memory. Accurate and predictive process modeling, in combination with virtual metrology enables the characterization of any feature on any given structure, is becoming a key requirement in advanced technology development. Virtual fabrication also accelerates the semiconductor development cycle, by substituting limited and lengthy wafer-based experiments with fast, large-scale virtual design of experiment. Several applications of virtual process modeling and metrology are illustrated in 3D NAND, DRAM, and logic technology. These applications include studies of 3D NAND pillar etch alignment (including tilt, twist, and bowing), DRAM capacitor process window optimization, advanced FinFET logic pitch-walking, and BEOL performance optimization. © *2023 Society of Photo-Optical Instrumentation Engineers (SPIE)* [DOI: 10.1117/1.JMM.22.3.031209]

**Keywords:** semiconductor; metrology; 3D NAND; DRAM; logic technology; BEOL; FinFET; pitch-walking.

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## 1 Introduction

All future semiconductor technology trends point to increased process and structural complexity,[1] which will lead to an increase in cost and development cycle time. Systematic structural defects created by this complexity are now a main factor in limiting successful yield-ramp.[2–4] Due to these trends, successful process integration has become an essential component in advanced technology development.

Technology development is driven by cycles of learning from earlier technology node development efforts. Next node development starts with what was learned at the previous node, and advances that node by developing process enhancements that provide performance improvements at an acceptable yield.[5,6] Typically, this learning is achieved by fabricating silicon development wafers using different process parameters, which is then followed by physical and electrical characterization of these wafers. The wafer processing usually takes 2 to 3 months per test batch, with subsequent characterization adding to the learning cycle time. Silicon-based learning and development is not only time-intensive but is also quite expensive due to high fab costs.[7]

A large portion of silicon-based process development and testing learning can be eliminated using predictive process modeling and virtual metrology.[8,9] Traditional TCAD modeling is useful for individual transistors, while *ab-initio* modeling is useful for novel materials and unit

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processes.[10] However, both approaches lack the necessary speed and large area modeling capability that is needed for predictive process development at advanced nodes. The use of virtual process modeling and metrology is also applicable to disruptive technology changes such as material changes or process flow changes that require fast turnaround understanding of any potential impacts to the process flow due to the disruptive technology change.[11–13]

In this paper, we demonstrate the ability of process modeling, 3D virtual wafer fabrication, and virtual metrology to gain insight into the most advanced technology logic and memory technologies. We start by examining a state-of-the-art 3D NAND structure[14] and its evolution from 96 tier stacks to 128 and beyond.[15] In our example, we demonstrate the advantages of using process modeling to replicate a 3D NAND HAR etch process. The HAR etch process is used to open tiny circular holes or channels from the top of the memory stack to the bottom, following the stack deposition process.[16] Virtual metrology can be used to virtually measure the channel hole CD variation from the top of the stack to the bottom of the stack, including tier alignment and twist and bow metrics.[17] These types of measurements are extremely difficult to measure using ordinary physical metrology tools.

Next, we look at an example of DRAM process modeling. DRAM devices have many of the same process complexities and metrology challenges that are encountered in other advanced technology nodes.[18] In this example, we examine the DRAM structure and its electrical metrics using virtual metrology, 3D design rule checks (DRC), and electrical characterization.[19] Using statistical process analysis, we also execute a design study using a DoE (design of experiment) to quickly and reliably identify the most critical process parameters. The results of our DoE are then used during process window optimization that provides an optimized process flow that maximizes the probability that critical process parameters to identify an optimum process flow that maximizes the probability that critical process parameters will fall within the process yield spec and result in a successful technology. Achieving this insight via virtual wafer fabrication and virtual metrology typically takes days, instead of the weeks to months required by silicon-based wafer development.

Finally, we review an example of how virtual fabrication and process modeling can be used in advanced FinFET logic development.[20] Advanced logic technology requires fin definition to be exact, with the fin width and pitch being identical across the entire chip. For many advanced logic technologies, the fin is patterned using a self-aligned quadruple patterning (SAQP) process;[21] other patterning processes such as EUV are also possible.[22] We demonstrate a model calibration technique for our virtual process model to define the required SAQP process including mandrel CD, spacer thickness, and etch bias and to ensure that our model is predictive of real-world results. The goal of this study was to eliminate pitch-walking, which is when manufacturing processes include a shift in the pitch value from one fin compared with a neighboring fin.[23] In our final example,[24] we use virtual fabrication to evaluate the performance of interconnects (line and via resistance, capacitance, etc.) across pitches using three different process flows: single damascene (SD),[25] dual damascene (DD),[26] and semi-damascene [subtractive metal (SM) etch].[4,27] The effects of process variation during the three flows are also investigated to determine the relative importance of process flow, variation, and scaling when moving toward aggressive pitch interconnects. The accuracy of these models is contingent upon developing a nominal model that describes the process flow as closely as possible. Calibration of each nominal model to hardware is critically important to be able to predict downstream process impacts due to technology evolution or disruptive process flow changes.

## 2 3D NAND

3D flash memory has essentially replaced two-dimensional (2D) flash as the state-of-the-art flash memory technology. Although 2D flash memory is lithography limited due to its traditional horizontal scaling, 3D flash memory scales in the $z$ direction by stacking multiple alternating layers vertically to achieve higher bit-densities.[28] These layers can number up to 96 or greater and need to be extremely uniform and defect-free.[29] Quantifying their uniformity and thickness is typically achieved with cross-sectional TEM, which is a destructive technique with throughput concerns. Reflectometry and ellipsometry both of which are indirect measurements and not

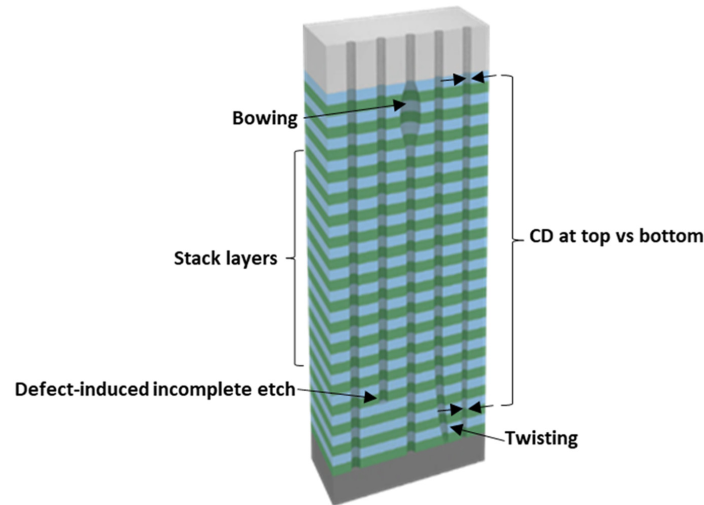



**Fig. 1** Simulated 3D cross-section showing stack deposition and potential HAR etch issues resulting from stack nonuniformity and defects.[31]

performed on every wafer and can also be used to quantify (and verify) layer uniformity and thickness.[30] Once a process is stable, the frequency of these metrology tests usually decreased resulting in missed screening of potentially yield-limiting uniformity issues and defects.

The most important physical feature of 3D NAND devices is the multi-layer architecture with high-aspect-ratio holes, including channel holes and contact holes. As 3D NAND technology matures, process and metrology challenges are shifting from lithography issues to film deposition and high-aspect ratio (HAR) hole etch control. Once stack deposition is complete, the HAR etch becomes a critical process step that requires unique metrology to measure and quantify the hole CD variation from the top of the 3D NAND stack to the bottom of the stack, as well as the hole alignment, twist, and any defect-induced bowing as, shown in Fig. 1.

The components and process step requirements of a typical 3D NAND technology are shown in Fig. 2. For demonstration purposes, the architecture that we use in our study is based on the terabit cell array transistor,[32,33] which has been reverse-engineered using the SEMulator3D® virtual fabrication software platform, using only publicly available information. The structural complexity and inherent 3D nature of this structure are ideal to demonstrate the value of a predictive 3D modeling platform. SEMulator3D® can be used to model the processes and

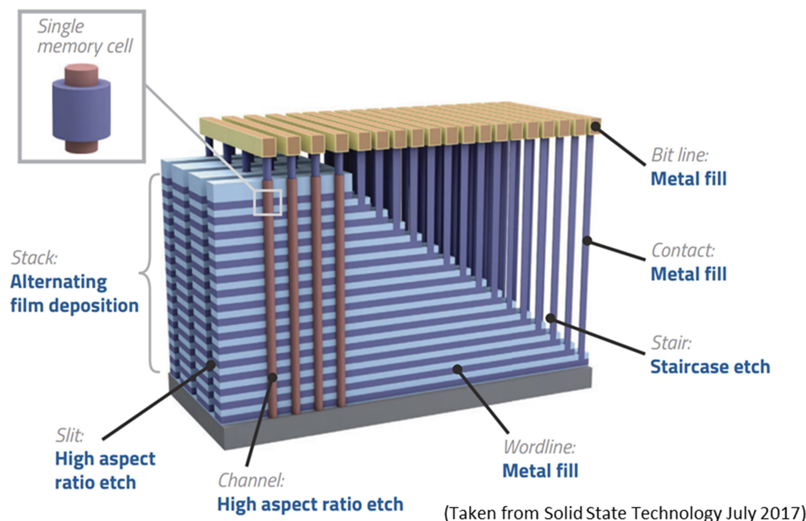



**Fig. 2** 3D NAND memory architecture showing some of the most challenging and critical deposition and etch processes, including the HAR-etched channel holes.[31]

generate the 3D structures shown in Fig. 2, and analyze, measure, and identify the source of potential 3D NAND structural problems (like those shown in Fig. 1). Using SEMulator3D®, we can virtually evaluate the effect of process variations during 3D NAND fabrication, particularly during channel etching and contact formation.

The HAR channel etch must be optimized for hole aspect ratios of 30:1 or more. Depending on the etch chemistry, high polymerization can result in sidewall tapering and prevent etch completion to the target depth. A key challenge of channel etching is to achieve appropriate polymerization, so the etch reaches the bottom contact without delivering excessive lateral etch bias at the top of the channel.[34,35] Quantifying the extent of hole CD variation and channel taper from the top of the channel to the bottom can be achieved with virtual process modeling and metrology as shown in Fig. 3. In Fig. 3, we model a stack of 32 alternating layers of oxide/nitride (∼1 $\mu$m deep) and calculate the channel area at the top and bottom of the channel as a function of the HAR etch process. We can evaluate the process window for the channel etch by using the result of a 180 run DOE that varies the stack etch taper, stack layer selectivity, and lateral etch bias of the stack. The resulting virtual metrology data highlight that a narrow process window is needed for this HAR channel etch [Fig. 3(a)]. For a nominal etch condition [Fig. 3(b)], the CD variation from the top to the bottom of the channel can readily be seen and numerically quantified. To ensure that the channel etch reaches the bottom contact, the sidewall angle for each stack layer must be >88 deg or the etch does not reach the bottom of the channel [Fig. 3(c)]. Finally, increasing the lateral etch bias in the polymer removal cycle can ensure that the etch reaches the channel bottom, but it comes at the expense of CD expansion at the top of the channel hole [Fig. 3(d)]. By incorporating this type of virtual metrology and statistical process variation, the process boundaries of various channel etch process parameters can be optimized prior to running excessive trial-and-error silicon wafers. This can reduce the number of silicon wafers used during the development process and can accelerate the timeframe of bringing technologies to market. Virtual studies can also be used to evaluate other channel etching schemes, such as those using bowed sidewalls or changing etch chemistry during mid-channel processing.[36]

In addition to having challenging etch process development issues, 3D NAND also uses challenging deposition processes. As previously mentioned, the stack deposition process must provide defect-free and uniform alternating layers, typically comprised of oxide and nitride. The deposition of many (typically 96 or more) alternating layers of oxide/nitride provides new challenges in defect reduction. With multi-layer film deposition, a small defect or particle embedded anywhere in the film stack can deform the layers above it such that the resulting surface topology

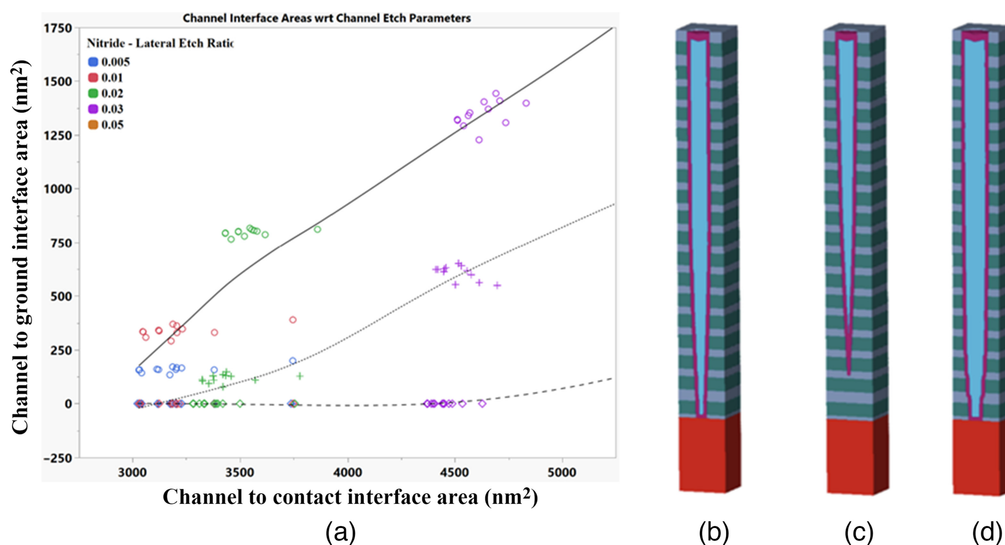



**Fig. 3** (a) Channel interface area at bottom versus top of channel. A channel interface area = 0 indicates that the etch stopped before reaching the bottom of the stack. (b) Nominal channel etch process showing tapering of channel hole. (c) Incomplete etch due to non-optimized etch taper angle. (d) Non–optimized etch resulting in CD "blowout" near the top of the channel.[15]

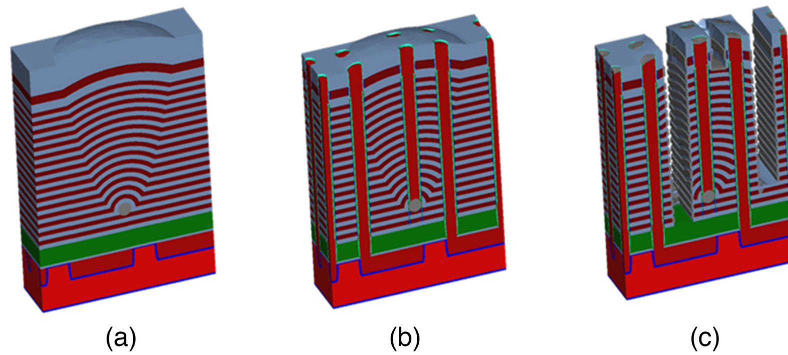



**Fig. 4** (a) A ~20 nm diameter defect embedded in the multi-layer film stack (32 stacks) magnified throughout the remainder of the stack deposition. (b) The defect is directly under the channel and blocks the etch, causing a bit-line failure. (c) Nonplanarity caused by a random defect affects "slit etch" later in flow.[15]

is no longer flat and uniform. When the embedded defect directly blocks the channel etch (or other HAR etches), it can wipeout an entire cell string [Fig. 4(a)].[37] A more insidious failure occurs when the embedded defect is not directly located in the path of a particular channel. In this case, the non-planar surface deformation can affect the etch depth of neighboring channel etches or word-line cuts, resulting in the failure of multiple cell [Fig. 4(b)]. Defects in stack deposition have received significant attention, resulting in defect reduction and improved film deposition processes. However, defect introduction can occur at many other points in the 3D NAND flash process flow and are extremely difficult to quantify with typical metrology techniques. Virtual defect insertion modeling can be used to evaluate the expected evolution of defects through the deposition process, making it significantly more manageable to locate, identify, and quantify these types of defects. For instance, the etch of the alternating film stack (oxide/nitride) after the word-line cut is a process that can create catastrophic failures. This process step can inadvertently insert residual metallic defect particles within the overhanging region of the film stack, resulting in device failure. Figure 5(a) shows a simple 20 nm defect placement within a region of interest in the structure and the subsequent impact on downstream metal-gate film deposition leading to an electrical break in the word-line [Fig. 5(b)]. The ability to virtually model such random defects and to quantify their location and morphology provides greater insight into measured yield impact and failures than is possible using test wafer production and standard metrology.

A final example of the complexities of 3D NAND processing and metrology is shown in the HAR etch of the channel film stack or tiers. In state-of-the-art 3D NAND, the number of tiers or

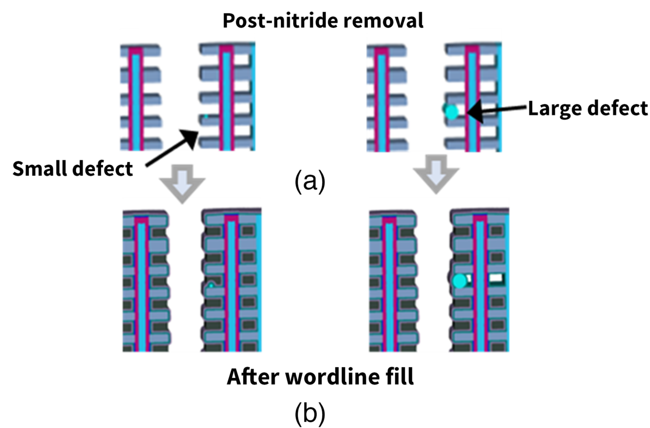



**Fig. 5** (a) A ~20 nm defect particle is placed after silicon nitride removal. (b) The subsequent metal-gate film deposition is blocked in the region of the defect, creating an electrical break in the word-line.[15]

material stacks (oxide/nitride or oxide/poly) exceeds 96 and is increasing with the introduction of every new node containing increased memory bit density.[38] As the number of stacks/tiers increases so does the aspect ratio of the required channel hole. The aspect ratio can be as large as 40:1 requiring significant etch process improvement as the number of tiers increase. Often the channel etch is done in two steps: a bottom stack etch followed by an upper stack etch. This two-step etch process can lead to misalignment between the upper and lower film stack. This can result in CD offset between the top and bottom of the stack as well as twist and bowing within the stack. Quantifying the stack misalignment, along with the twisting, and bowing is extremely difficult using standard metrology tools since it is a destructive process. Using 3D process modeling and virtual metrology, these stack features (pre and post etch) can be readily quantified.

Figure 6(a) shows an upper and lower multi-tier stack containing alternating post-etch layers of oxide and nitride. The depiction of the two stacks highlights the potential misalignment when multitier stacks require two etches to successfully etch the entire stack. This misalignment can lead to an offset between the top and bottom CD of the channel. The offset is extremely difficult to quantify with conventional metrology. Using virtual metrology, however, we are able to quantify this offset as shown in Fig. 6(b). Virtual metrology can be used to quantify the offset by creating two virtual masks and measuring their offset via a 3D structure search. This can quantify both the offset and the tilt angle.

Figure 7 shows the measured CD at various locations in the stack as a function of etch tilt angle. With virtual metrology, we can measure the channel CD anywhere within the structure. In Fig. 7, we have highlighted top CD, mid CD, and bottom CD for illustration purposes. Using virtual process model, the etch process can be modified by changing the tilt angle of the etch and any polymer redistribution during etch. These virtual process changes will ultimately change the shape of the channel. The variation of etch tilt angle can also have an impact on channel bow as well. Figure 8(a) shows the variation of tilt angle and its impact on the location and magnitude of the channel bow. The virtual process simulation enables accurate top and bottom etch tilt angle modeling, as well as metrology that can determine the inter-relationship between the critical etch parameters and the location and magnitude of both the channel CD and bow.

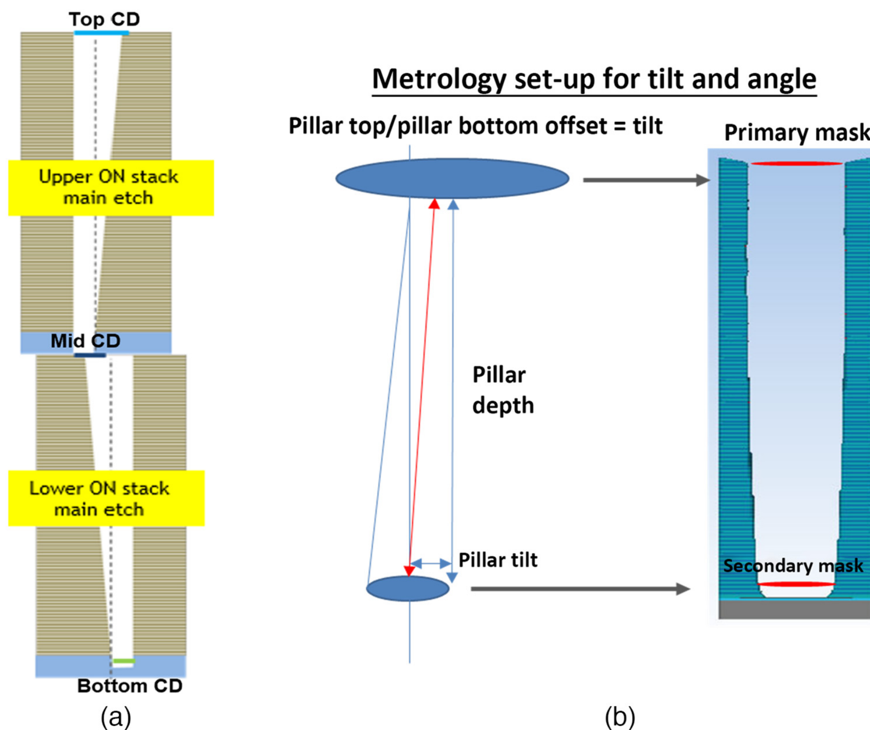



**Fig. 6** (a) Top and bottom tier misalignment, showing tilt angle and CD. (b) Metrology setup for tilt and top/bottom channel offset measurement.

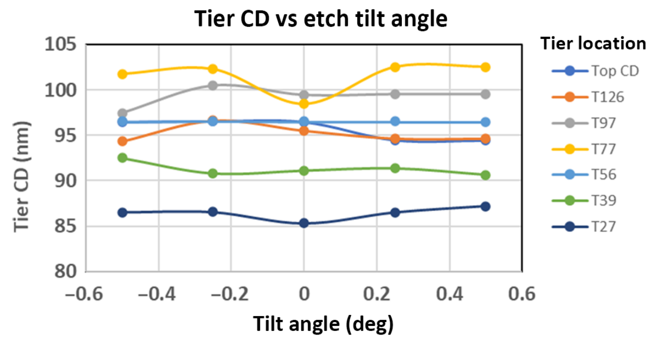



**Fig. 7** Measured CD at various locations in the stack as a function of etch tilt angle.

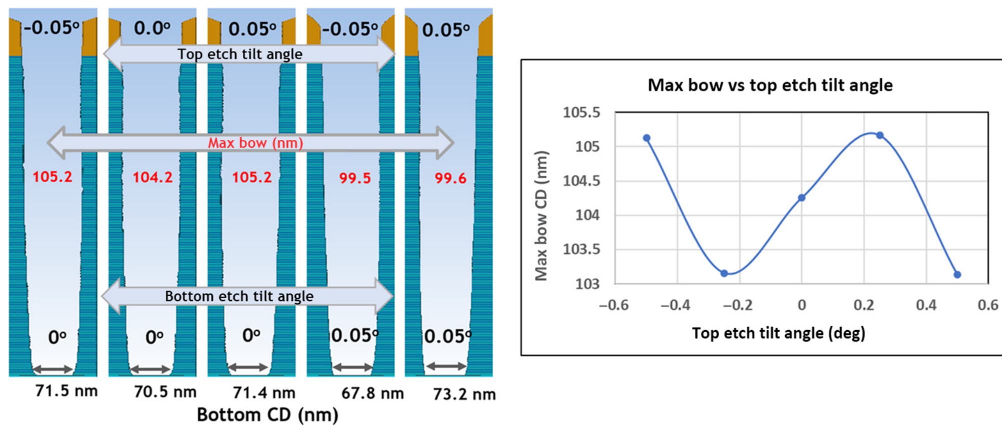



**Fig. 8** Virtual metrology results showing the variation of tilt angle and its impact on the location and the magnitude of the channel bow. The tier CD at various locations in the channel versus etch tilt angle.

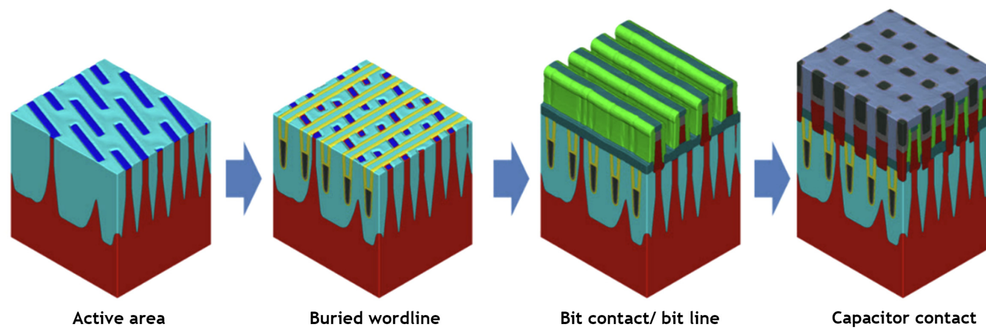



**Fig. 9** Example DRAM process flow from AA through CC.[19]

## 3 DRAM

Advanced DRAM technology has many of the same process complexities and metrology challenges encountered in advanced 3D NAND technology.[39] We now examine an example of an advanced DRAM structure and process flow using virtual wafer fabrication. The process flow and structure shown in Fig. 9 was developed using publicly available data and consists of a

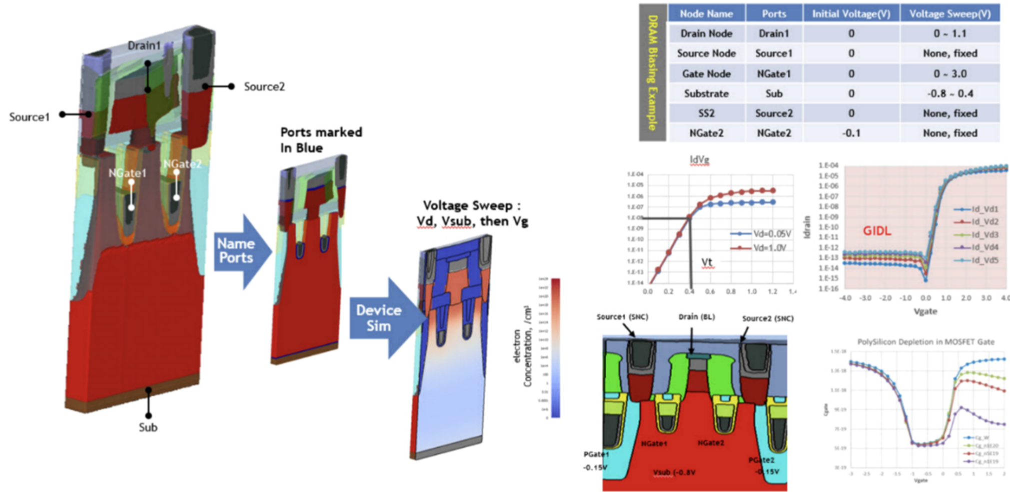
Fig. 10 (a) Virtual metrology results showing trench top CD and other critical structural metrics. (b) Results of structure search (3D DRC) showing contact area between CC and AA.[19]

28-nm active area (AA) pitch, buried word-line, and 44-nm bit-line pitch. The model has been constructed up to the end of the capacitor contact (CC), to enable electrical analysis and subsequent cell optimization through execution of a DoE and sensitivity analysis. We also review the results of a process window optimization[40] that was undertaken to provide optimized POR values for each process parameter. Our goal in this study was to maximize the percentage of critical process parameters that keep us within the desired yield specification.

SEMulator3D® allows the addition of two kinds of geometrical metrology. The first is virtual metrology, which allows the measurement and verification of model structures. The second is structure search, which is a 3D DRC that examines the entire 3D model (or a portion of the model) to identify measurement extremes and their values and physical location in the model. Structure search can include measurements such as line widths and contact areas, and count material components. These types of measurement are very useful in determining if the magnitudes and locations of geometric excursions change due to specific process variations. Figure 10(a) shows a 3D cross-section of the DRAM trench and the resulting virtual measurements of top trench CD and other critical structural parameters of the DRAM device, including the AA spacer dimension of the SAQP process. These virtual metrology measurements would normally require destructive measurements to accomplish using real silicon wafers. Figure 10(b) shows the interface area between the CC and the AA. The process model highlights the interface area [Fig. 10(b), area in blue] and identifies it as a device failure point.

Another type of analysis that can be undertaken with our process model is electrical device simulation. Once the process model is created, the modeling software can identify device ports and electrodes in the 3D structure and simulates the electrical characteristics of the DRAM device using physics-based models of temperature, bandgap, and electron/hole mobility. Important device parameters can be automatically extracted, such as threshold voltage (Vth), sub-threshold slope (SS), drain-induced barrier lowering, and ON current (Ion). Furthermore, AC electrical analysis is utilized to extract junction capacitances and the field dependent SRH and band-to-band tunneling currents for the gate-induced drain barrier lowering (GIDL) phenomenon. Using the same software platform, all of this can be accomplished while simulating the effect of 3D process changes on electrical performance. Figure 11 shows the complete modeling flow from 3D structure through port/contact definition and the resulting electrical bias sweeps, including drive current versus gate bias, threshold voltage (Vt), GIDL current, and AC capacitance as a function of gate bias and doping level.

Being able to measure and quantify important process and device parameters during simulation is critical if you want to accurately correlate simulation results to actual wafer results.[12] Once accurate correlation is achieved, we can then establish a nominal process model that can be used to study statistical process parameter variation and its impact on actual cell operation. For example, we use the built-in analytics capability of SEMulator3D® to study the effects of DRAM wordline (WL) process variation on device electrical performance. We performed a 200 run Monte Carlo analysis to study the effect of DRAM word line (WL) variation and its impact on threshold voltage (Vth). In our study, the WL process parameter values are set randomly, using a Gaussian distribution around a mean value and standard deviation. This type of WL variation study, if performed with real wafers, would require hundreds of experiments and



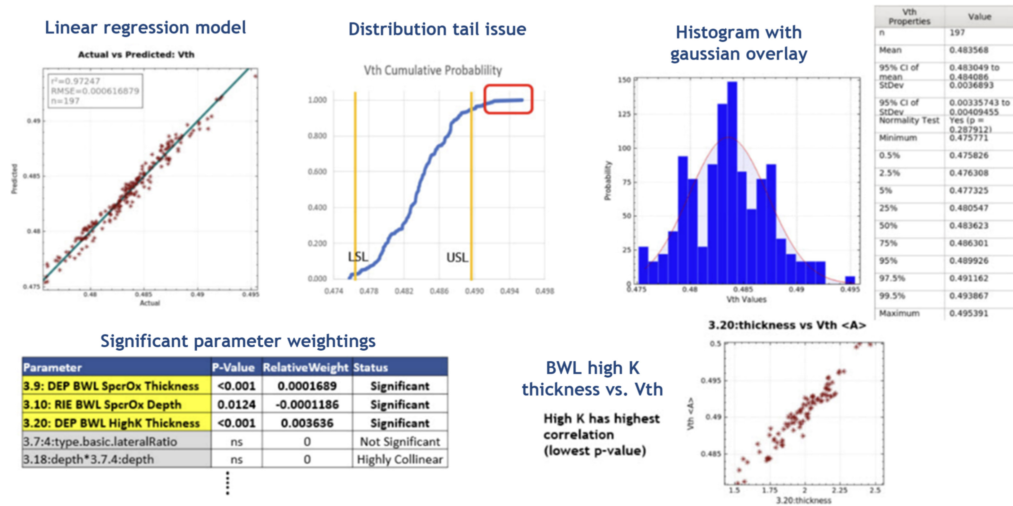

| Node Name | Ports | Initial Voltage(V) | Voltage Sweep(V) |
|---|---|---|---|
| Drain Node | Drain1 | 0 | 0 ~ 1.1 |
| Source Node | Source1 | 0 | None, fixed |
| Gate Node | NGate1 | 0 | 0 ~ 3.0 |
| Substrate | Sub | 0 | -0.8 ~ 0.4 |
| SS2 | Source2 | 0 | None, fixed |
| NGate2 | NGate2 | -0.1 | None, fixed |

**Fig. 11** SEMulator3D® identifies device electrodes in a 3D structure and simulates device characteristics as in TCAD, but without the need for time-consuming TCAD modeling.[19]

take months of process time. Using process simulation, it can be completed in a matter of hours or days.

The results of our DoE are shown in Fig. 12. In the DoE trials, the threshold voltage Vth was varied between 0.48 and 0.5 V. A regression analysis helps identify three parameters that have significant impact on Vth. The three most significant factors identified for further examination are the spacer oxide thickness, WL spacer etch depth, and the gate dielectric thickness (obviously the most significant parameter).

As a final step to optimize the DRAM cell, we identified specific electrical characteristics that are required for peak DRAM performance. In our example, we focused on the WL threshold voltage (Vth) and defined the optimal target value as 0.482 V. The DoE experiment identified the most important process parameters that influence the variation in this electrical parameter. The goal now is to perform process window optimization that identifies the optimal values for each of these important process parameters. The results of the process window optimization will be a set of process parameter values that deliver optimized electrical characteristics for maximum yield and cell performance. The SEMulator3D® process window optimization capability can provide




| Vth Properties | Value |
|---|---|
| n | 197 |
| Mean | 0.483568 |
| 95% CI of mean | 0.483049 to 0.484086 |
| StDev | 0.0036893 |
| 95% CI of StDev | 0.00335743 to 0.00409455 |
| Normality Test | Yes (p = 0.287912) |
| Minimum | 0.475771 |
| 0.5% | 0.475826 |
| 2.5% | 0.476308 |
| 5% | 0.477325 |
| 25% | 0.480547 |
| 50% | 0.483623 |
| 75% | 0.486301 |
| 95% | 0.489926 |
| 97.5% | 0.491162 |
| 99.5% | 0.493867 |
| Maximum | 0.495391 |

| Parameter | P-Value | RelativeWeight | Status |
|---|---|---|---|
| 3.9: DEP BWL SpcrOx Thickness | <0.001 | 0.0001689 | Significant |
| 3.10: RIE BWL SpcrOx Depth | 0.0124 | -0.0001186 | Significant |
| 3.20: DEP BWL HighK Thickness | <0.001 | 0.003636 | Significant |
| 3.7:4:type.basic.lateralRatio | ns | 0 | Not Significant |
| 3.18:depth*3.7.4:depth | ns | 0 | Highly Collinear |

**Fig. 12** Results of SEMulator3D® DoE Monte Carlo runs. The analysis identifies the most important process parameters impacting the WL threshold voltage. The analysis also identifies corner cases in the tail of the distribution.[19]

**Table 1** New mean values identified resulting in improved % in-spec yield.[17]

| | Initial | | After process window optimization | |
|---|---|---|---|---|
| Parameters | Mean (nm) | Std. dev. (nm) | Mean (nm) | Std. dev. (nm) |
| Spacer Ox thickness | 21.439 | 0.50 | 21.870 | 0.50 |
| Spacer Ox etch | 27.701 | 1.00 | 26.740 | 1.00 |
| High-*k* thickness | 1.931 | 0.20 | 1.832 | 0.20 |
| % in-sec | 34.7 | | 50 | |

**Table 2** Reoptimized standard deviation of high-*k* thickness variation resulting in improved % in-spec yield to 89.3%.[17]

| | Initial | | After process window optimization | |
|---|---|---|---|---|
| Parameters | Mean (nm) | Std. dev. (nm) | Mean (nm) | Std. dev. (nm) |
| Spacer Ox thickness | 21.439 | 0.50 | 21.870 | 0.50 |
| Spacer Ox etch | 27.701 | 1.00 | 26.740 | 1.00 |
| High-*k* thickness | 1.832 | 0.20 | 1.832 | 0.13 |
| % in-spec | 50 | | 89.3 | |

a prediction of maximum yield for a given set of processes under consideration and redefine nominal process conditions and variation control requirements to achieve acceptable yield.

In our example, the targeted Vth is set to 0.482 V with a success criteria of $+5\ \mathrm{mV}/-5\ \mathrm{mV}$. The three critical process parameters determined from the DoE (Fig. 12) are then set to their nominal values. The standard deviation of the three process parameters are shown in Table 1. We then modify the nominal values of the three important process parameters and review the effect of these changes on % in-spec yield for Vth. The result of our process window optimization study is an increase in the in-spec yield of achieving the targeted Vth from 34.7% to 50%. Subsequent optimization of the standard deviation of the most important of the three process parameters, namely, the high-K thickness, results in an even more dramatic increase of the in-spec yield from 50% to 89.3% (see Table 2). These results demonstrate that a dramatic improvement in overall yield can be attained by controlling the mean and standard deviation of specific process parameters and related equipment settings. This type of analysis also provides process integration engineers with valuable insight and direction in establishing an optimal process recipe. This insight and direction can be obtained by only hours of simulation, and without the months of wafer processing that is normally required. Using process modeling, an optimal set of process parameters can be established quickly and early in development, establishing a direction for subsequent wafer processing and testing.

## 4 Logic Technology

Advanced logic technology has evolved from planar structures to 3D structures, similar to memory technology.[41,42] The core components for any logic technology are the front-end-of-line (FEOL) which defines the device structure and the back-end-of-line (BEOL) which includes the wiring levels which connect numerous devices together to form circuits. The middle-of-line (MOL) which focuses on contacts between FEOL and BEOL is equally important but we do not discuss MOL in this paper.

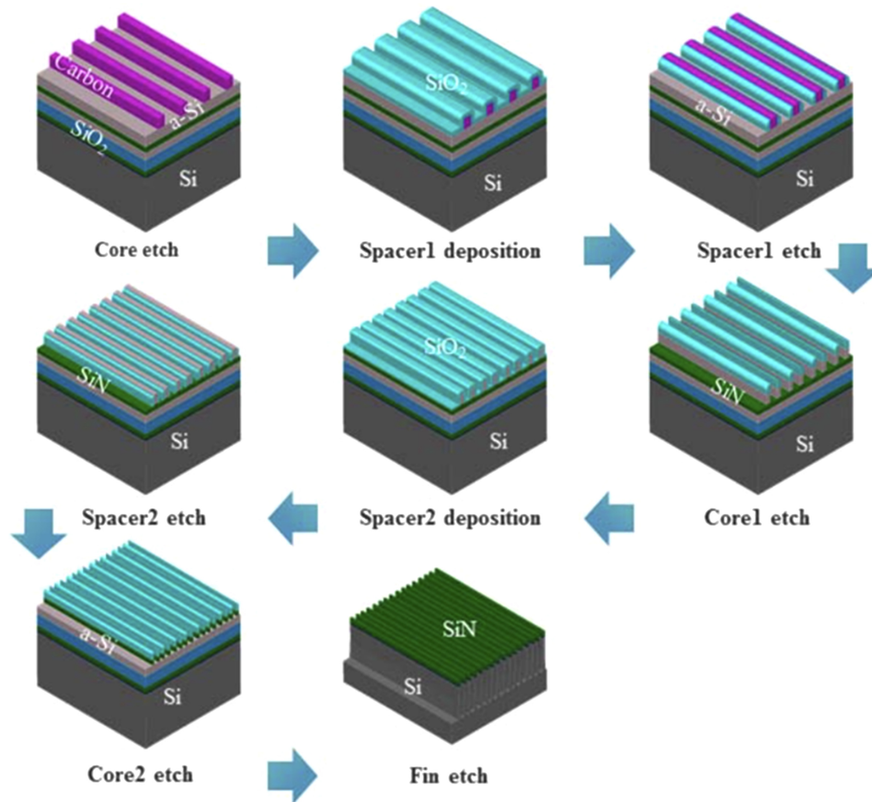



**Fig. 13** Process flow for SAQP fin patterning.[23]

## 4.1 *Fin Pitch-Walking*

In our first example of using virtual process modeling and virtual metrology, we focus on the process technology that defines the FinFET fin device structure, namely, SAQP.[43] The SAQP process flow is shown in Fig. 13. Mandrel lines (typically carbon) are patterned and an oxide spacer1 is deposited and etched, followed by mandrel removal via chemical etching. The remaining spacer acts like a hardmask for the dry etch of the underlying amorphous silicon (a-Si) layer. A second spacer is then deposited and etched, and the pattern is transferred into the silicon substrate quadrupling the original pitch of mandrels.

The goal is to define a uniform pattern of fins, separated by shallow trench isolation, as shown in profile in Fig. 14. These fins ultimately define the FinFET structure. It is important that the fins have similar widths and are equally separated, so the device characteristics are uniform across the wafer. This occurs when the fin spacing parameters $\alpha$, $\beta$, and $\gamma$ are equal across the device (Fig. 14). When the SAQP process is not optimized, or when $\alpha$, $\beta$, and $\gamma$ are not equal, the pattern of fins can suffer from "pitch-walking."[44] The extent of pitch-walking is defined by $\mathrm{MAX}(\alpha,\beta,\gamma) - \mathrm{MIN}(\alpha,\beta,\gamma)$. The result of fin pitch-walking is shown in Fig. 15, where the variation in fin height between the fins is readily apparent. This difference in fin height results in nonuniform device electrical characteristics.

Quantifying the extent of pitch-walking and determining the critical process parameters that control it is extremely important and typically requires significant wafer-based testing. With virtual process modeling and metrology, the key process parameters that control the fin width and spacing, namely, the mandrel CD, the deposited spacer oxide thickness, and the spacer etch bias can be varied and the effect of this variation can be quantified. The impact of these key process parameters on pitch-walk can be systematically characterized by running a full-factorial DoE and determining their optimal values. As shown in Fig. 15, SEMulator3D® can display a 2D (top) view of the simulated silicon surface, and virtual metrology can be used to predict the min/max fin spacing CD of this simulated surface. This enables a reliable measurement of fin pitch-walk for any process variation simulated.

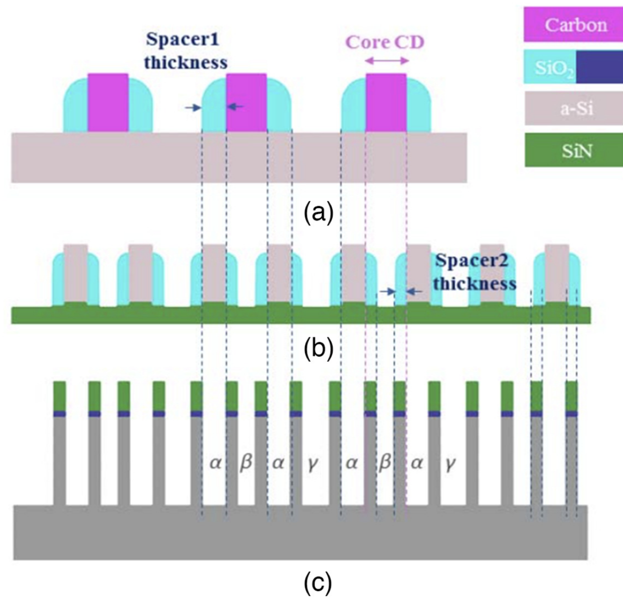



**Fig. 14** Cross-section of (a) spacer1 etch, (b) spacer2 etch, and (c) fin etch also defining the spaces between fins.[31] The STI is not shown here.[23]

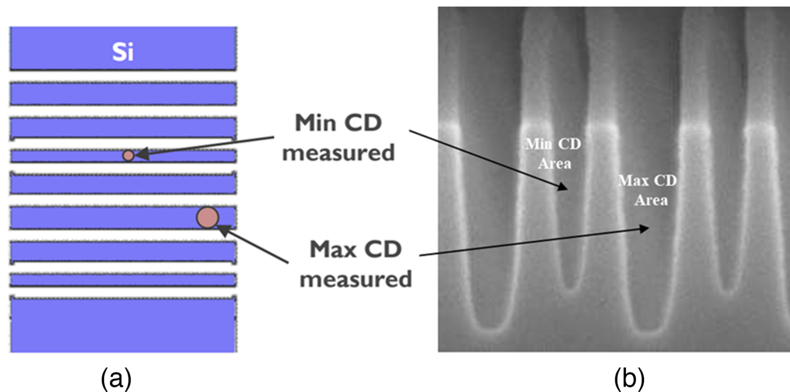



**Fig. 15** (a) Top view of fin area postpatterning showing min and max spacing between fins. (b) TEM showing result of fin pitch-walking where fin height and spacing vary causing non-uniform device electrical characteristics.[23]

Virtual process modeling and metrology can provide a comprehensive assessment of how SAQP process parameters changes impact fin pitch-walking without ever having to process and characterize a single wafer. The results of a full-factorial process model DoE can be used to optimize the spacer1 and spacer2 thickness for a fixed mandrel (core) CD as shown in Fig. 16. In Fig. 16, the spacer1 and spacer2 thicknesses are varied around their nominal value by 25% and the mandrel line CD is varied by −2 nm from its nominal value. The amount of pitch-walk is shown in Fig. 16 as a function of spacer1 and spacer2 thicknesses. For a mandrel CD of 33 nm, the pitch-walk is at a minimum for spacer1 and spacer2 thicknesses of 15.0 and 9.25 nm, respectively (black triangle in Fig. 16). For a spacer thickness variation of 1 nm around its nominal value, the pitch-walk remains reasonably small. At a larger spacer thickness variation, the pitch-walk rapidly increases to >14 nm (corner cases). This amount of pitch-walk would result in no spacing between the fins.

The DoE results also display the impact of mandrel CD on spacer thickness variation. When the mandrel CD is reduced from 33 to 31 nm, the pitch-walk dependency on spacer thicknesses is unchanged, but the optimum point is shifted. The optimal spacer1 thickness now increases from

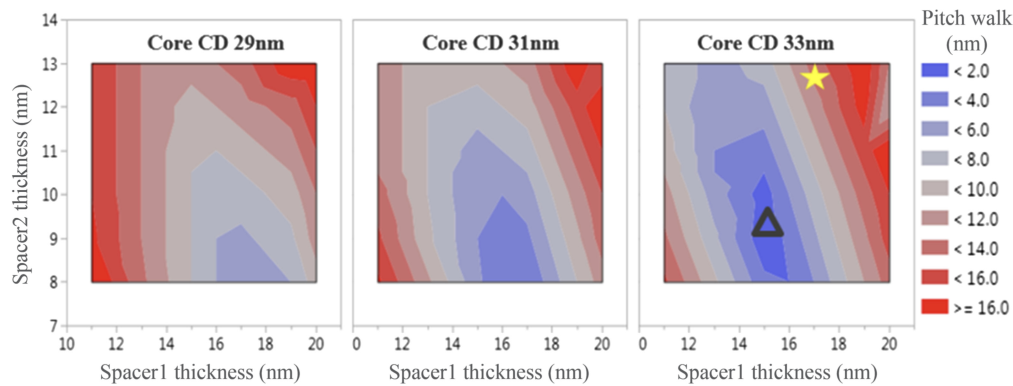



**Fig. 16** Pitch-walk calculated from analytical model as a function of spacer1 and spacer2 thickness for various mandrel (core) CD. Nominal starting process condition is shown by the yellow star. (Taken from Ref. 23).

15.5 to 17 nm and the spacer2 thickness is reduced by ∼1 nm. For a mandrel CD of 29 nm, the minimum pitch-walk is obtained for even larger spacer1 and smaller spacer2 thicknesses. The results of this virtual metrology and statistical analysis indicate that in this range of mandrel CD values, the minimum pitch-walk is ∼2 nm and that the spacer process window must be well-controlled to avoid pitch-walking. The merits of virtual process modeling coupled with virtual metrology and statistical process variation are clearly demonstrated in this fin pitch-walking analysis. Further optimization of the SAQP process parameters, such as the mandrel CD taper angle, can also be performed to minimize fin pitch-walk.[23] It is important to note that this type of process optimization requires no wafer starts and can be performed in days as opposed to months of processing time and cost required using wafer-based testing.

## 4.2 *BEOL Optimization*

As logic technology has scaled to smaller dimensions, interconnects have become the dominant source of delay in integrated circuits, surpassing even the transistor itself.[45] There is significant ongoing work focused on mitigating the impact of interconnects on delay, including the exploration of alternate materials and integration schemes. We used SEMulator3D® to model the interconnect performance of three alternate integration schemes and their scaling behavior.[24] The virtual process models for the three integration flows were able to accurately capture the correct geometric and spatially dependent material properties. The objective was to identify which of the three integration schemes enabled the best interconnect performance at future smaller pitches. The three integration flows were:

- SD, where the via is etched and filled in a separate interlayer dielectric (ILD) prior to trench ILD deposition, etch, and metal fill.
- A hybrid-metallization scheme that uses the standard DD patterning approach including a self-aligned via for perfect via alignment every time. The trench is filled with a traditional barrier, liner, and Cu.
- SM scheme, also called semi-damascene, where a blanket metal film is deposited, and lines are formed therein. This allows for lower Cu resistivity through the formation of significantly larger grains in the annealed blanket film than in confined trenches, thus reducing grain-boundary scattering contributions to the resistivity.[8] However, the drawbacks of this approach are that Cu is hard to etch (used here instead of Ru for comparison to the other flows) and a blanket film adds complication to alignment steps because it covers the entire surface of the wafer and therefore any alignment markers that may be in use.

The results of this work identified the advantages of each integration flow from an RC and via resistance point of view. The model also included secondary effects of BEOL patterning such as line edge roughness (LER)[46–48] and considered the impact of EUV lithography and

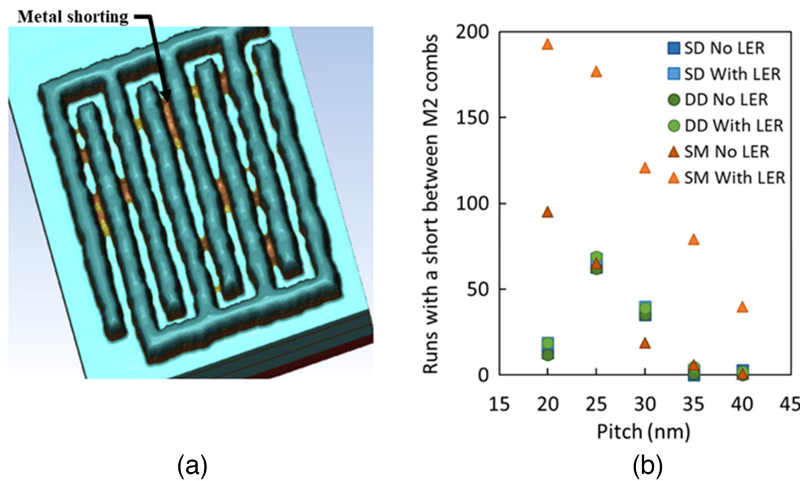



**Fig. 17** (a) Shorting in the SM M2 structure when LER is present and (b) number of DOE runs having shorts between M2 combs across pitches and with versus without LER. (From Ref. 24).

EUV + self-aligned double patterning (SADP) required to achieve sub-30 nm pitch. From these results, all three integration approaches were shown to be relatively equivalent. However, utilizing the virtual metrology capabilities of the software, it was also shown that shorting between metal lines can develop at the smallest dimensions. Figure 17 displays a top-down view illustrating an example of shorting between two M2 combs in the SM scheme when LER is present. We also plotted the number of runs where shorting is observed between the M2 combs for all three integration approaches (right). It was demonstrated that the SM flow has significantly higher rates of shorting than either damascene flow, particularly in the presence of LER. This is likely due to the inverse line profile of the SM approach compared with either damascene flow. Both damascene processes result in a more uniform metal line width from the top to the bottom of the line, whereas the SM process results in a more tapered line profile at the bottom of the line which can restrict the metal etch process at small pitches and result in residual metal shorting between lines. This is another excellent example of using virtual metrology to quantify advantages and disadvantages of specific metallization schemes without having to fabricate a single wafer.

## 5 Conclusions

The challenges of developing advanced semiconductor technology increase with every node. Both memory and logic technology are adversely affected by both process complexity and decreasing dimensional scale of each advancing node. The standard model of fabricating, waiting, and then testing chips is an extremely time-consuming and costly endeavor. In this paper, we provide an alternative to this standard model by demonstrating the robust capabilities of virtual process modeling and virtual metrology. The merits of this approach are shown in the complexity of etching and characterizing HAR 3D NAND channels, including the quantification of tilt, twist, and bowing, and to the control of advanced logic FinFET pitch-walking. We demonstrated the ability of the SEMulator3D® virtual wafer modeling platform to create highly accurate and predictive process models and showed how to use these models to quantify all necessary geometrical and electrical metrology, including statistical variation. With this capability, technology developers can predict the impact of process variation on yield and can gain insight into the specific process steps that improve or degrade performance.

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