

Development of an InGaAs SPAD 2D Array for Flash LIDAR

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ABSTRACT

An InGaAs Single-Photon Avalanche Photodiode (SPAD) array and a hybrid photon-counting image sensor have been developed for time-resolved applications in the near infrared region, especially for Flash LIDAR. The implemented array has a 100 μm pitch 32×32 matrix, and the active area in each pixel has a diameter of 12 μm . A dedicated read-out IC incorporates an active quenching and recharge circuit, and an in-pixel time-to-digital converter with 318 ps resolution for providing stable Geiger-mode operation of the InGaAs SPAD pixels and a simultaneous time-resolving function. The uniformity of the electrical field in the entire two-dimensional area is one of the key characteristics as it affects most performance parameters. The breakdown voltage mapping revealed the SPAD array has an excellent uniformity. Full characterizations of dark count rate, photon detection probability, and timing jitter were performed and will be discussed. Methods of suppressing afterpulses were examined by utilizing an adjustable hold-off function. The results showed that the function worked effectively to reduce the afterpulse probability. Finally we prove that the InGaAs SPAD image sensor has the capability of accurate timing detection for constructing a flash LIDAR in the near future.

Keywords: Indium Gallium Arsenide (InGaAs), Single-photon avalanche diode (SPAD), Hybrid structure, Time-to-digital converter, Flash LIDAR

1. INTRODUCTION

In the last decade, there has been intense interest in Single-Photon Avalanche Diodes (SPAD) and numerous studies regarding all aspect of both sensors and circuits have been examined in order to establish single-photon sensitivity, precise timing resolution, and the integration of SPADs onto standard CMOS technologies with fine dimensions. These researches can be classified into two categories: one is how to implement SPADs into the target process technologies, while another aspect is how to implement processing circuitries with high timing accuracy like time-to-digital converters [1]. However, there were difficulties developing SPADs which had higher sensitivity in the near-infrared region due to the too shallow depth that prevented implementation of a wide depletion region. To produce a high fill-factor is also difficult because the complex circuits occupy most of the pixel area.

One of our objectives to implement SPADs is to provide photon counting capability in the near-infrared region and is to apply it to time-resolved applications, such as a flash LIDAR. In order to solve these problems, we reported the concept of the hybrid SPAD image sensor by employing a Through-Silicon-Via (TSV) technique which leads the signals from the front-illuminated sensor to the backside and enables staking it on the read-out IC (ROIC) [2]. This technique allows more flexible designs for both the sensors and the ROIC to apply the best technology we can choose. Recently, we have developed other SPAD sensors in Silicon which have higher sensitivity in the wavelength range of 600 – 900 nm compared to the standard products [3]. By combining these new sensors and the ROIC, hybrid SPAD sensors with higher sensitivity in the near-infrared region can be provided. However, further extending the near infrared sensitivity would be hard to implement in Silicon.

On the other hand, the SPAD sensors based on III-V compound semiconductors especially InGaAs were also studied for applications such as remote sensing, 3D integral imaging and so on, while focusing on enabling sensitivity from near-infrared to shortwave-infrared [4]. The effective circuit implementation methods to operate the compound semiconductor sensors were also studied [5]. Therefore, we started to implement a flash LIDAR by InGaAs SPAD sensors.

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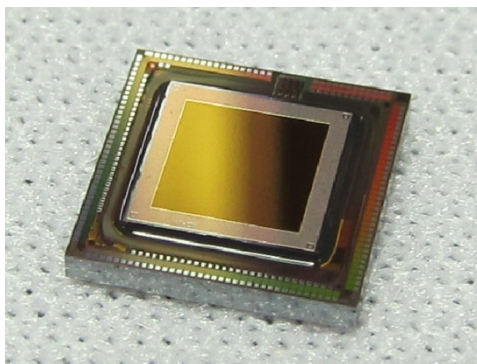
This manuscript is organized in the following topics. The overall implementation method for the InGaAs SPAD image sensor, the block diagram of the designed read-out IC and the brief description for each component are discussed in section 2. To provide time-of-arrival detection of the incoming photons by a two-dimensional plane simultaneously, the delay line based pixel-level TDC was designed. The characterization was performed particularly for the fine resolution detection and these characterization results are summarized in section 3. In section 4, we review the performance of the InGaAs SPAD array in Geiger-mode operation. The fundamental parameters regarding dark count rate (DCR), photon detection probability (PDP), timing jitter and afterpulse probability were examined.

2. IMPLEMENTATION OF INGAAS SPAD IMAGE SENSOR

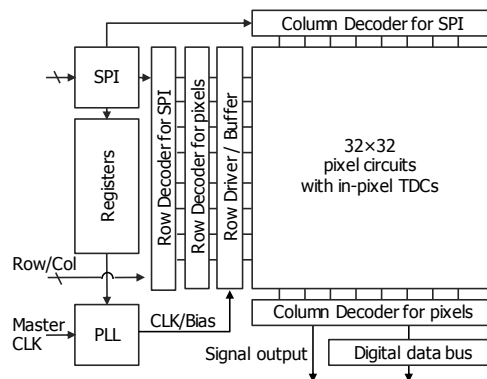
2.1 InGaAs SPAD image sensor and hybridization onto ROIC

Unlike the CMOS monolithic single-photon avalanche photodiode array, several techniques to enable each component of the hybrid image sensors were required. Figure 1(a) shows the appearance of the developed chip consisting of the InGaAs SPAD array with 100 μm pitch 32×32 pixels, and the CMOS read-out IC (ROIC) designed in a 0.18 μm standard CMOS technology. The detailed structure of the InGaAs SPAD sensor is described in section 2.2. Interconnections between the sensor array and the ROIC were realized by flip-chip bonding techniques. Although several options to form the micro bump electrodes could be selected, for instance solder bumps, indium micro bumps were applied in this work. An underfill material was dispensed at the gap between the sensor and the ROIC to provide mechanical reinforcement and prevention from failures.

Flash LIDAR is one of the ranging techniques, and the required functionality for the ROIC is the simultaneous detection of the time-of-arrival of the laser pulses in the entire two-dimensional area. For this sake, the time-recording function was needed for each pixel circuitry. Therefore an in-pixel time-to-digital converter (TDC) was designed. The entire architecture of the ROIC is drawn in Figure 1(b). The ROIC consists of the 32×32 pixel circuits, a decoder for row and column selection, a data output bus, a serial peripheral interface (SPI) and related circuits, and a phase-locked loop (PLL). The PLL provides a base clock frequency and a control bias propagated globally in the pixel array in order to sustain the characteristics of the in-pixel time-to-digital converters. Since several control signals (not shown) in addition to the row and column addresses were required for the ROIC operation, an FPGA on the evaluation board was used to provide the control signals and to collect the output data. A signal output line was equipped and it could be used for direct monitoring of a frontend circuit on a pixel when the row and column addresses are defined. The schematic of the pixel circuit is drawn in section 2.4. The signal line was used for characterization summarized in section 4.



(a)



(b)

Figure 1. Outline of the hybrid InGaAs SPAD image sensor. (a) The appearance of the image sensor comprised of the 32×32 pixel array and the read-out circuit (ROIC). The stacked chip was hybridized by a flip-chip bonding technique and the underfill material was filled around the bumps in the gap between the sensor and the ROIC. The dimension of the ROIC is $6.28 \times 6.28 \text{ mm}^2$. (b) The architecture of the read-out IC designed in the 0.18 μm CMOS technology.

2.2 Structure of InGaAs SPAD and spectral response

In order to realize the Flash LIDAR at near-infrared and shortwave infrared wavelengths, a dedicated InGaAs SPAD sensor array was designed. InGaAs photodiodes are one of the III–V compound semiconductor devices and are widely used for near-infrared detection because of the low bandgap value of 0.73 eV at room temperature. However, fabricating an InGaAs single-photon avalanche photodiode had further challenges because its depletion region had direct absorption process, lower ionization coefficient of both α (electrons) and β (holes), and larger ionization coefficient ratio of $k = \beta/\alpha$ compared with these parameters of Si devices. Due to its lower bandgap energy, dark current larger than Si devices is induced by the thermal generation process. Therefore, the absorption layer and the multiplication layer were separated. The absorption layer is designed to absorb photons and generate electron-hole pairs, and subsequently the multiplication layer accelerates the carriers to initiate impact ionization when a large reverse bias voltage is supplied. This is the so-called separated absorption and multiplication (SAM) structure. When a bias below its breakdown voltage (V_b) is applied, the diode acts as a linear-mode avalanche photodiode. And its multiplication factor (M) is limited to several tens. However, once the bias exceeds its V_b , the avalanche photodiode starts a further cascade process of the avalanche buildup which brings a large number of carriers reaching up to ten to the power of 5 or 7 of multiplications. In this way, the InGaAs devices are sensitive to a few photons.

The cross-section of the developed InGaAs SPAD and the spectral response are shown in Figure 2(a) and (b) respectively. The measurement was performed with a large diameter device (200 μm dia.) at the conditions of $M=1$ and room temperature. The composition ratio of the absorption layer was fabricated to provide the sensitivity at 1.55 μm , and the cutoff wavelength was 1.69 μm . The 32×32 SPAD array was designed with a diameter of 12 μm in the active region and 100 μm pitch. To prevent the optical crosstalk between neighboring pixels and to block the surface leakage current, an isolation trench was implemented around each active area.

To confirm the performance of the developed 32×32 array, several ways to measure its characteristics can be considered. Confirming the sensitivity profile is one of the methods to verify the design of the fabricated sensors. In this work, a laser sweep in Geiger-mode operation by using a laser head ($\lambda=1.537 \mu\text{m}$, pulse width = 46 ps) and a light collection optics to concentrate the laser spot was examined to estimate the electrical field formation. During the laser sweep with 4 μm steps, the number of output pulses was monitored by the signal output line and a universal counter (53220A, Keysight). Figure 3 shows the obtained profile in three pixels at the conditions of $T = 255 \text{ K}$ and $V_e = 1.05 \text{ V}$. The profiles showed that each pixel was sensitive within the designed active diameter of 12 μm and the edge breakdown was not observed. These results suggested the electrical fields were formed uniformly across these pixels. Moreover, the range of photosensitivity was limited to the designed active area, and the other regions showed almost no sensitivity due to the isolation trench. Full characterization for the uniformity of the entire 32×32 array was performed by collecting the breakdown voltage in each pixel, and the results are reported in section 4.1.

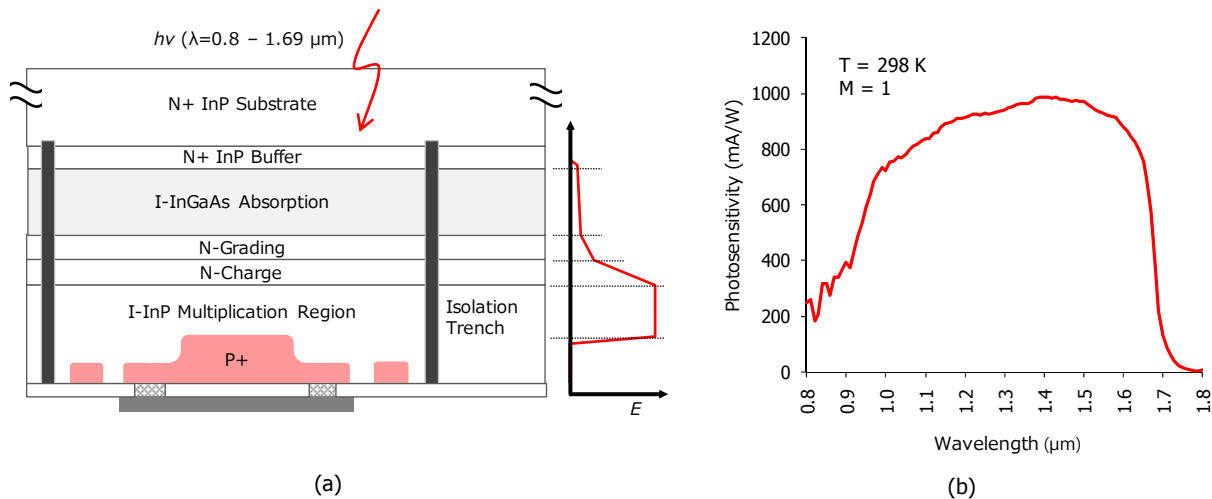


Figure 2. Implementation of the InGaAs Single-Photon Avalanche Photodiodes. (a) The cross-section of a pixel's layer composition and the electrical field profile. (b) Spectral response in the developed InGaAs SPAD. The measurement conditions were room temperature and no bias ($M=1$). The measurement was performed by a large device with a diameter of 200 μm .

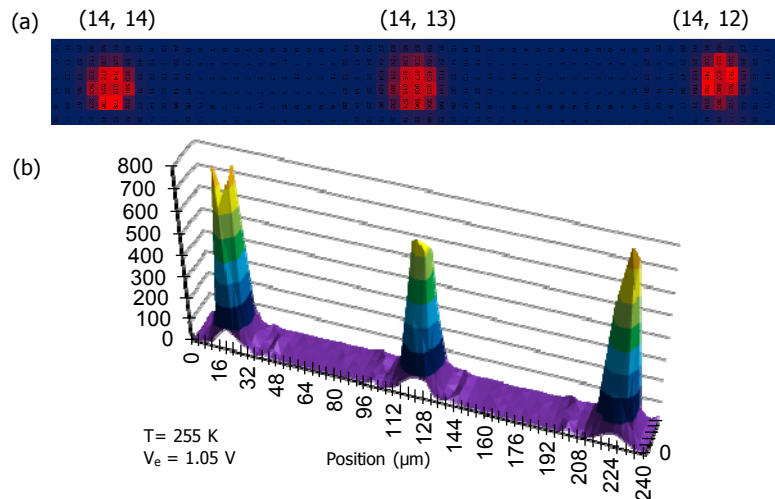


Figure 3. Sensitivity profile swept by a laser. (a) Top view of the photoresponse of three pixels in the 32×32 array by measuring pitch of 4 μm. (b) Perspective view of the relative sensitivity profile.

2.3 Implementation of pixel circuit

In order to process the Geiger-mode operation and the simultaneous time-recording function, a 100 μm pitch pixel circuit was designed. Figure 4 shows the layout image of the pixel circuit which incorporates an active quenching and recharge circuit (AQC) including a 1bit SRAM, a control logic for the TDC control, a delay line based fine interpolator, a 16-to-4 encoder, a coarse counter, and finally memory cells and output gates. A bump pad for interconnection to the SPAD is also equipped (not shown) on the top of each pixel. An active quenching and recharge circuit is common technique to provide stable control for Geiger-mode operation, and one of the objectives is a pulse width shortening to enhance the maximum count rate, and the other objective is discharging carriers as much as possible to suppress afterpulses. In the latter purpose, the pulse width should employ longer values rather than short ones. More detailed explanations regarding the frontend circuit are given in section 2.4. The in-pixel TDC consists of the control logic, the delay line, the encoder, and the coarse counter. Since the delay line has 16 stages, the encoder translates the 16 stage signals to 4 bit output. A global clock (CLK) line is equipped and propagated to all of the pixels in a row, and the CLK provides typically 200 MHz frequency to the coarse counters through the logic circuits. By feeding the STOP signal from outside the pixel, a time-interval measurement is finished, and then, the latched data are stored in the memory and are read out pixel-by-pixel. A more detailed explanation and an operation sequence are shown in section 2.5.

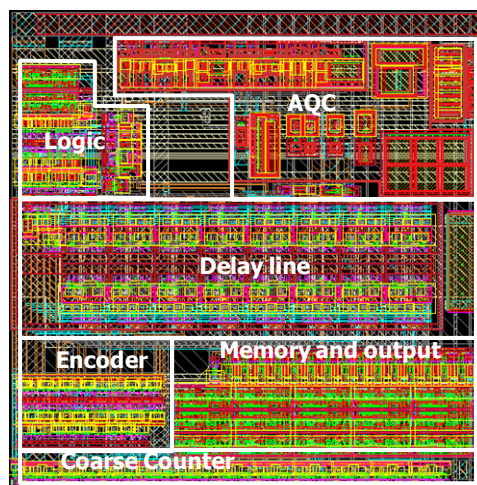


Figure 4. CAD layout image of each pixel circuit. Top metals including the bump pad are turned off to show the circuit blocks. The designed area is 100 × 100 μm².

2.4 Functionality of frontend circuit

Figure 5(a) shows the schematic of the frontend circuit. Once the avalanche current is discharged and flowed into the NMOS-based quenching resistor, the voltage of the bump pad node starts to rise. Because the threshold detection should be matched with the characteristics of the SPAD sensor, a comparator instead of a simple inverter was selected to meet the possible excess bias of the SPAD by adjusting the threshold level. When a voltage pulse at the bump pad reaches to the threshold voltage V_{th} , the comparator converts the voltage pulse signal to a digital pulse. Immediately after the digital pulse is generated, the PMOS transistor M_1 is activated and the bump pad node goes to a high level, and this behavior is an actively quenched state. The digital pulse is fed into both the control logic circuit for the TDC as outputs of the frontend circuit and the hold-off duration adjustment circuit. The hold-off duration can be determined by an external bias V_{delay} , and the adjustment circuit detects whether the pulse width has reached the required value or not. When the pulse width has reached the set point, the shutdown transistor M_1 is inactivated and subsequently the reset transistor M_2 is activated. A slight temporal gap was kept between the inactivation of the M_1 and the activation of the M_2 to prevent both transistors turning on simultaneously and not to flow a large penetrating current. With the activation of the M_2 transistor, the SPAD is recharged actively. In order to suppress the large dark count rate and the afterpulse, the hold-off duration can be adjusted by V_{delay} , and the range of the adjustable duration is 10 ns to 800 ns. Figure 5(b) summarizes a sequence of these operations. A 1bit SRAM circuit is also equipped beside the AQC, and the address select signal and the data line is connected. The SRAM can be used for the individual pixel shutdown by accessing via the SPI. The ARM is also an external signal provided by the FPGA or other instruments to control the pixel activation and inactivation. In this current design, the ARM signal is common in all 32×32 pixels.

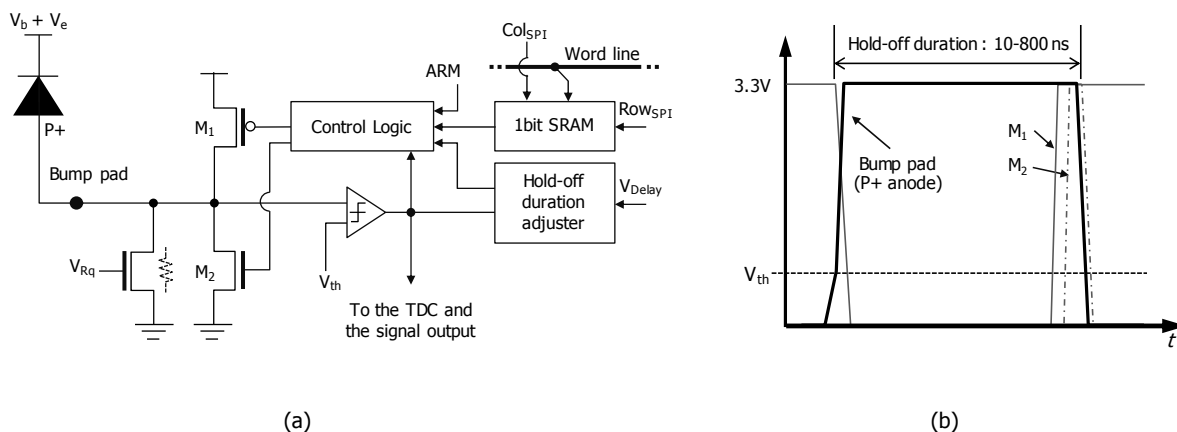


Figure 5. Schematic and operation principle of the frontend circuit. (a) The block diagram of the active quenching and recharge circuit (AQC). (b) The operation principle of the AQC. The thick solid line represents the voltage change of the bump pad node to be manipulated. The thin solid line represents the applied pulse form onto the gate of M_1 , and the dashed line represents the signal for M_2 gate.

2.5 Design of In-Pixel Time-to-digital converter

Various implementation principles are known to achieve precise time measurements by time-to-digital converters. Since almost all power consumption of the read-out IC is subject to the pixel circuit design, the in-pixel TDC is the dominant contributor to the power dissipation. For conflicting issues that need to minimize the power dissipation while keeping the required temporal resolution, a current-starved inverter based delay cell was employed. Figure 6(a) shows the entire structure of the in-pixel TDC. The delay line based interpolation circuit is comprised of 16 stage delay cells, and a single unit is shown in Figure 6(b). The delay cell contains two stage current-starved inverters, analog switches, and a reset PMOS transistor. When the delay line is activated, the signal path in a series of the delay cells is opened by the signal S, while the data latch path is closed by SB. On the other hand, when the delay line is stopped, the signal S is inverted, and the chain of the delay cells is intercepted. A small inverter helps the determination of the node D status. In this manner, the defined state of the node D on each stage is transferred to the encoder which translates the 16 stage signals into a 4 bit binary code.

The propagation delay of each delay cell is maintained by the control bias connected to the current starved inverter. The value of the delay could be tuned from 200 ps to 600 ps in 250 K, and the values were chosen with respect to the power consumption. For fixing the delay value during a measurement, a compensation scheme by the global PLL was implemented. Figure 7 shows the block diagram of the global PLL. The 8 stage delay line is employed as the voltage-controlled oscillator (VCO). In this work, the VCO runs with 200 MHz frequency typically. The frequency can be varied by the multiplication factor of the programmable counter and the reference clock. The reason why the half delay line is used as the VCO is as follows: the measurable range on the delay line in the pixel is calculated by 312.5 ps per stage and 16 stages; therefore, the full range to be interpolated is 5.0 ns. During the 5.0 ns period, a positive edge pulse runs through the delay line. Since the coarse counter evaluates the period defined by the global clock, the elapsed time between the positive edges should be covered by the period in which the pixel delay line can interpolate.

In this way, the PLL provides the global clock and the control bias generated by the low pass filter (LPF). These lines are connected to buffer amplifiers in the row driver circuit, and then, propagated to each pixel.

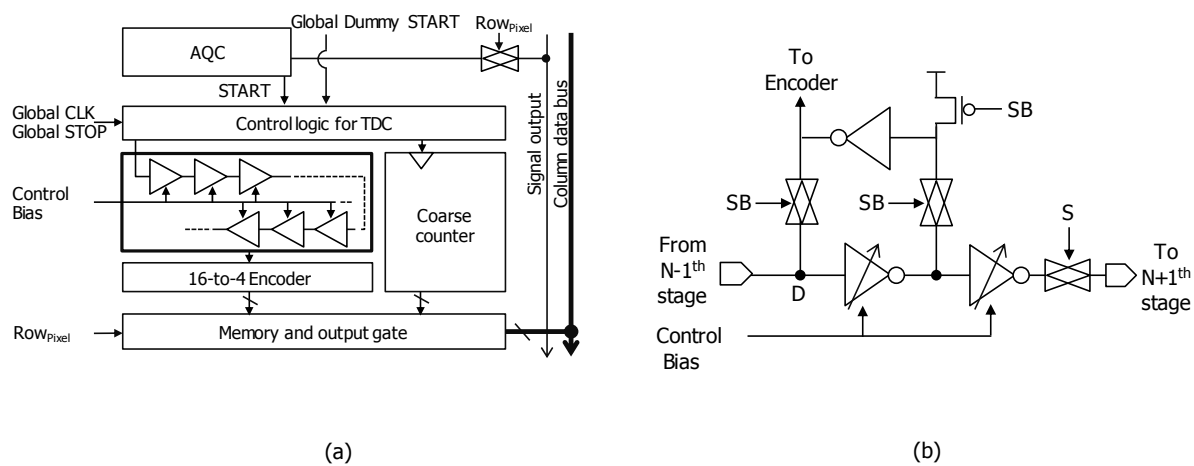


Figure 6. Schematic diagram of the in-pixel TDC. (a) The block diagram of the in-pixel TDC. The AQC shown in Figure 4 is simplified. The output from the AQC has a branch to the signal line and the control logic for the TDC. To evaluate the TDC without the sensor, a dummy START signal is also connected into the logic circuit. (b) A single unit of the delay cell in the 16 stage fine interpolator.

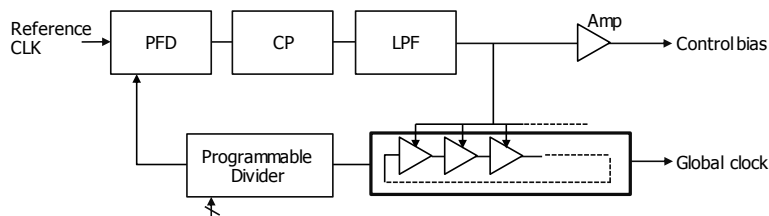


Figure 7. Block diagram of the phase-locked loop. It consists of the phase-frequency detector (PFD), the charge pump (CP), the passive low-pass filter (LPF), and the programmable divider. The half-length delay line was implemented as a voltage-controlled oscillator (VCO) to provide 200 MHz global clock. The control bias adjusted at the LPF is copied and distributed to each pixel.

By employing the described circuits, the time interval measurements can be performed. Figure 8 summarizes the operation sequence, and two measurement cycles are shown. At first (T1), the signal synchronized with a laser source is generated. When photons impinge into the SPADs, the AQCs are activated and generate the START signal to the control

logic (T2). Soon after receiving the START signal, the delay line starts the propagation of a positive pulse. When the rising edge of the global clock is detected at the control logic (T3), the propagation of the delay line is frozen and its states defined. Subsequently the global clock is fed into the coarse counter (T4) which measures the coarse interval defined by the global clock, and it is continued until the global STOP signal is injected (T5). And finally, the TDC and the control logic are reset (T6). So the TDCs turn to the waiting state to receive events. By this sequence, the time interval (T_{meas1} , T_{meas2}) between the photon detection and the STOP pulse can be determined. Since the period between the light source signal and the STOP signal is defined by users, the target period ($T_{target1}$, $T_{target2}$) can be calculated.

The conversion sequence is initiated by the impinging photons. The circuits are never activated unless photons or dark signals are generated. Therefore, reducing dark count and afterpulse is another important factor to optimize the image sensor's power dissipation. Once the event happens and the time data is recorded, the results are stored into the local memory circuits, and the readout of the pixel memories is performed in the sequence of 1024 pixels. The entire data capturing cycle depends on the read-out speed.

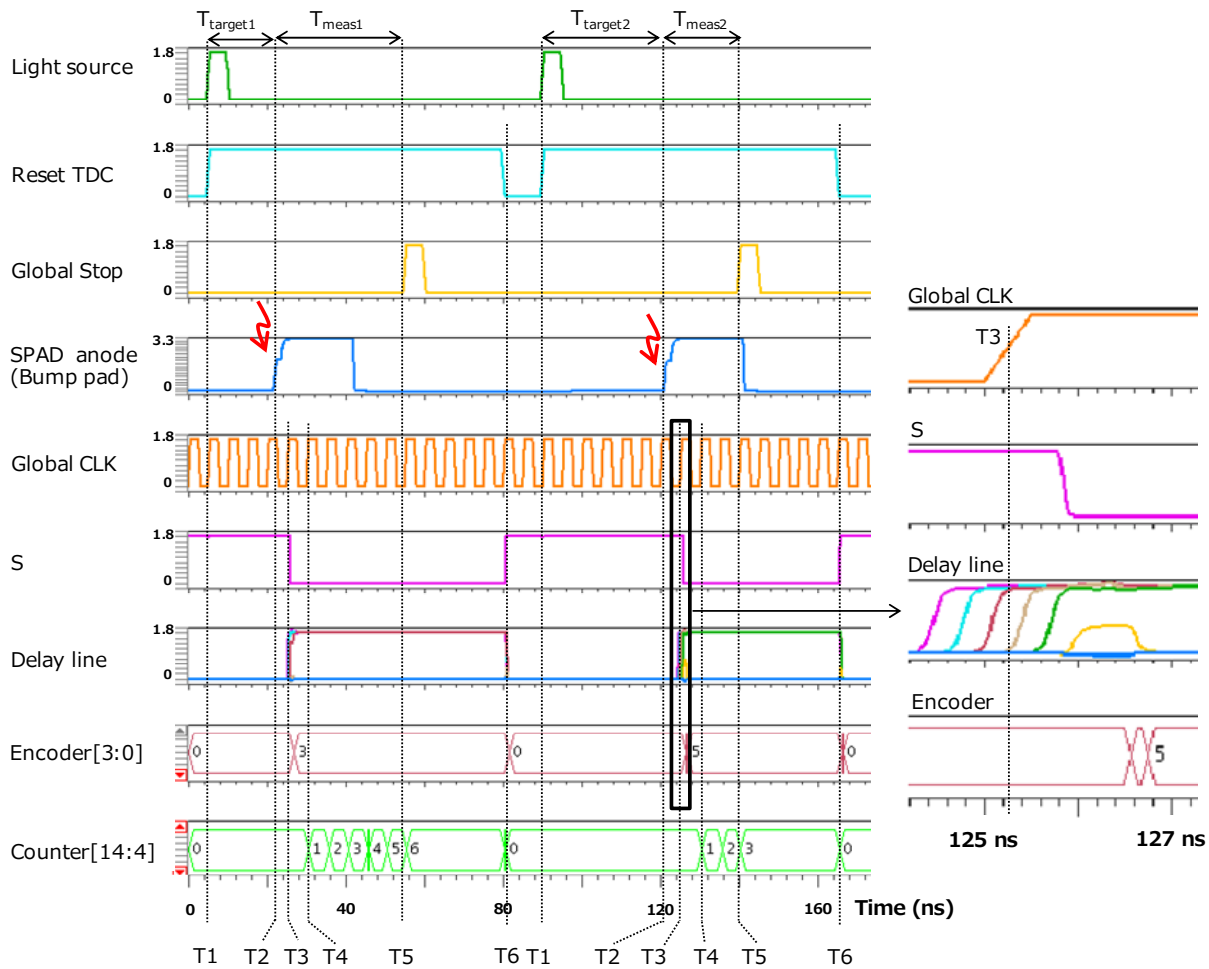


Figure 8. Conversion sequence of time measurements. This figure explains the two independent cycles to show the entire control of the key components. The signals related to the readout sequence are not shown. The details at T3 are shown in the right figure. In this simulation, the resolution of a single stage was 312.5 ps.

3. CHARACTERIZATION OF IN-PIXEL TDC

3.1 Performance of the in-pixel TDC

The intrinsic timing resolution of the in-pixel TDC without the SPAD sensors was characterized. For these measurements, the ROIC is equipped with the dummy START signal port to access the control logics, and the dummy signal can be fed by external instruments or FPGAs for debugging the in-pixel TDCs. Since the dummy START signal is common in the 32×32 pixel circuits, the evaluation for each in-pixel TDC can be done in parallel. In order to characterize the resolution of the TDC, the high precision delay generator (DG645, Stanford Research Systems) was used. The control signals to operate the ROIC was provided by the FPGA, and the dummy START signal was connected through the delay generator which could provide delayed pulses with 10 ps steps. The measurements were performed in the conditions of the PLL's frequency of 187.5 MHz and the single stage delay of 333 ps.

Figure 9 shows the stair plot with 10 ps sweep of an in-pixel TDC. The Y axis value consists of the 4 bit fine interpolator code and the low-order 2 bits at the coarse counter. In accordance with the delayed pulses, the TDC outputs were decreased in the stepping manner. A plateau was observed in the range of 1.5 ns to 2.2 ns. This was caused by a shortage of the delay line length, and it suggested the delay value of the single stage was faster than expected. Based on the stair plot, the resolution on each stage was calculated and the results are shown in Figure 10. The fluctuation among stages was observed suggesting the deviation of stray capacitance loads in each stage. Due to the plateau, the resolution value of the 15th code becomes 900 ps, and this failure will be fixed in the next revision. Except the 15th code, the average value of the actual resolution per stage was approximately 318 ps and the standard deviation was approximately 54 ps.

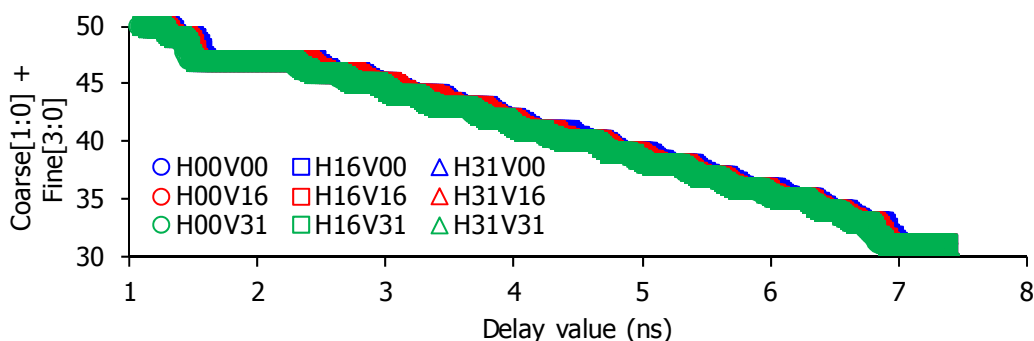


Figure 9. Responses of the fine interpolator with 10 ps step sweeps at the typical pixels in the 32×32 array

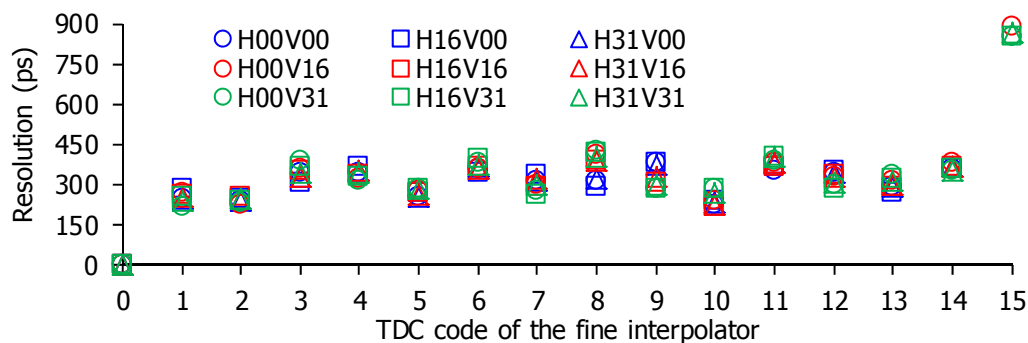


Figure 10. Resolutions of each stage in the fine interpolator at the typical pixels

3.2 Performance of the global PLL

The timing jitter of the global PLL affects the overall performance of the in-pixel TDCs because the coarse counter is driven by the propagated global clock. The timing jitter was confirmed by the fast oscilloscope and its value was 53.6 ps. Since the reference clock provided by the FPGA had some jitter also and the value was 25 ps, the intrinsic jitter of the PLL was calculated as 47.3 ps.

4. CHARACTERIZATION OF INGAAS SPAD ARRAY

4.1 Breakdown voltage distribution

The term *uniformity* is one of the important words which express the characteristics of sensors, however it has multiple uses because it can be applied regarding the breakdown voltage, the dark count rate (DCR), the photon detection probability (PDP) and other parameters. Although the uniform sensitivity across the individual active area is very important for appropriate characteristics in Geiger-mode operation, the uniformity of the breakdown voltage across the two-dimensional array is the first fundamental step to evaluating performance because the high voltage to the cathode is supplied commonly and the high voltage cannot be changed independently in each pixel.

The breakdown voltage measurements were performed and the results are summarized in Figure 11(a). Since the pixels were each connected to a pixel circuit, the way of measuring I-V curve like a single channel device could not be applied. Therefore, the bias sweeps around the breakdown voltage on each pixel were performed. When the applied high voltage reached at least its breakdown, the SPADs started to emit pulses through the frontend comparator. Since the pulses could be monitored via the signal output line, we determined the breakdown voltage at the bias condition where rectangular pulses started to be emitted. In this way, the overall distribution of the V_b was mapped. The result shows that a very smooth distribution has been obtained across the 32×32 array. Due to a small mistake in the sensor array design, a small gradient of increasing its breakdown value from the bottom to the top was observed. We think this is such a severe problem, so improvements will be made in the future devices. Figure 11(b) shows the histogram of the breakdown voltage. The full-width at half maximum (FWHM) of the distribution was 292 mV even though the V_b had the gradient.

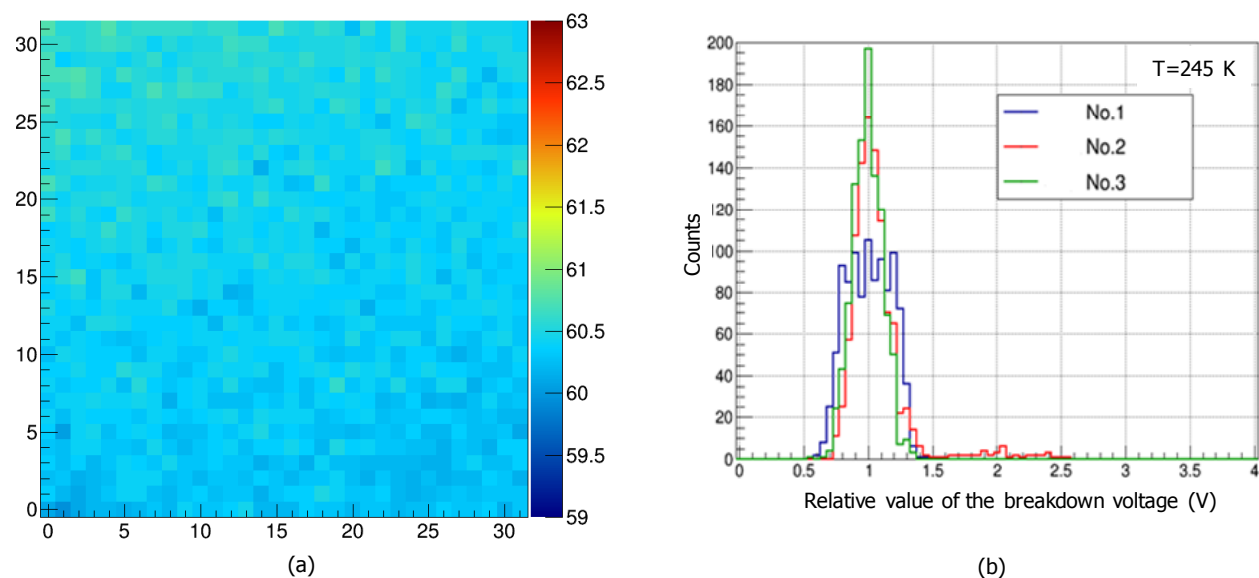


Figure 11. Distribution of the breakdown voltage across the 32×32 pixel array in the condition of $T = 245$ K. (a) Two-dimensional map. The color bar represents the value of the breakdown voltage. (b) Histogram of the breakdown voltage. Three samples were compared and showed almost similar distribution.

4.2 Afterpulse probability

A fraction of the dark count rate which contributes greatly to measurement noise comes from the afterpulse phenomenon. Although the afterpulse is seen in Si SPAD devices, it is also dominant in InGaAs SPAD sensors. This phenomenon occurs when a portion of carriers generated by an original avalanche trigger are trapped in the deep-level traps in the depletion region, and then are released after a certain period and reactivate the avalanche buildup. The Geiger-mode operation is known to emit binary pulses no matter what carriers trigger the avalanche multiplication. Therefore, it would be difficult for users to distinguish the original pulses and the afterpulses. Moreover the lifetime of the deep-level trap could last as long as several μ s to several tens μ s.

Afterpulse probability can be estimated by measuring its autocorrelation function. In order to measure the autocorrelation, an accumulation of pulse interval periods was collected by employing the histogram function on a high

speed oscilloscope (WaveMaster 808Zi-A, Teledyne LeCroy). As described in section 2.3, the frontend circuit has the functionality to adjust the hold-off duration which is aimed to reduce the afterpulse probability by restricting recovery from the quenched state of the SPAD's diode to permit trapped charges to be emitted out of the depletion region. Figure 13 shows typical examples of the results obtained in the series of PDP measurements in three conditions regarding the pulse width in a fixed excess bias and stable temperature. While the non-correlated fraction was distributed in the regular manner which could be fitted by a single exponential function by the assumption that the random distribution obeyed a Poisson process, the correlated counts were observed within 3 μs . The ratio of these fractions could be calculated by the curve fitting by two-exponential function (1), and the results were 86.4%, 50.8%, and 14.2% in accordance with the pulse width of 25 ns, 200 ns, and 800 ns respectively. These measurements were performed in $V_e = 1.9 \text{ V}$ and $T = 251 \text{ K}$.

$$f(t) = e^{p_0+p_1t} + e^{p_2+p_3t} \tag{1}$$

The trends resulting from different hold-off duration periods were examined along with the excess bias V_e and the results are shown in Figure 12. It clearly shows that the shorter hold-off duration brings significant afterpulse while the longer duration has afterpulse probability. The PDP mapping discussed in section 4.4 was measured with not only the PDP value but also the afterpulse probability pixel-by-pixel, and the PDP map shown had the afterpulse fraction subtracted.

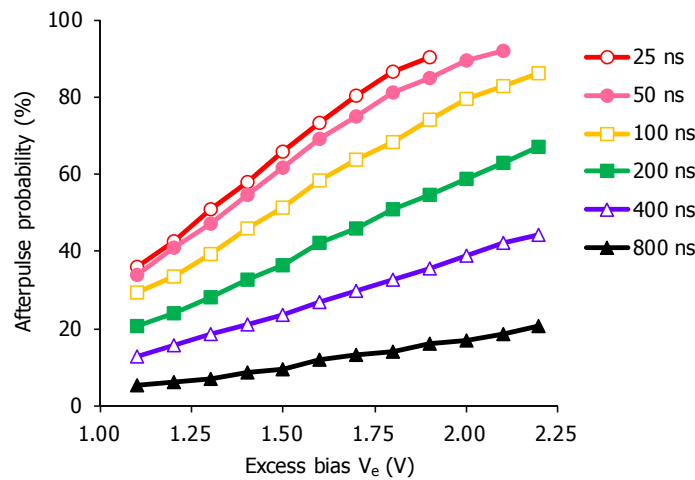


Figure 12. Trend of the afterpulse probability as a function of the V_e with the various pulse width conditions

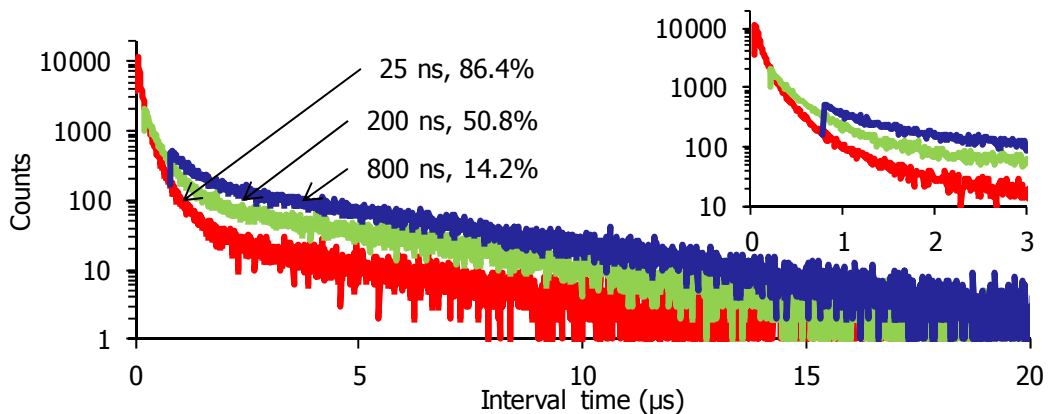


Figure 13. Autocorrelation function of inter pulses in the range of 20 μs for an individual channel of the 32×32 SPAD array with different pulse width conditions in the fixed excess bias $V_e = 1.9 \text{ V}$, $T = 251 \text{ K}$. The inset shows the details within 3 μs . The indicating labels represent the pulse width condition and the afterpulse probability respectively.

4.3 Dark count rate mapping and analysis

The dark count rate (DCR) is known as one of the most important noise sources in SPADs. The reason is that it limits not only the lowest level of the signal detection, but also measurable intervals in which the phenomenon of interest can be evaluated, for instance, time-of-flight of the flashed light. While DCR for individual pixels should be as low as possible to achieve ideal devices, uniformity across the entire two-dimensional array is another important aspect to be realized. The DCR mapping across the whole 32×32 pixels at $T = 242$ K was performed and the result is shown in Figure 14. Because the evaluated SPAD array tended to increase its breakdown voltage from the bottom to the top edge, the distribution of the DCR also had the gradient in the map. However, the distribution of the DCR can be marked as an almost smooth surface which means the SPAD array had uniform characteristics. A small number of pixels exhibited a large DCR. Figure 15(a) shows the DCR distribution as a function of the pixel population. The inset of Figure 15(a) is the detail at the range of over 96% of the population. The analysis showed 99% of the pixels have the DCR below 350 kHz at $T = 242$ K. Figure 15(b) shows the distribution of the DCR as a function of DCR value.

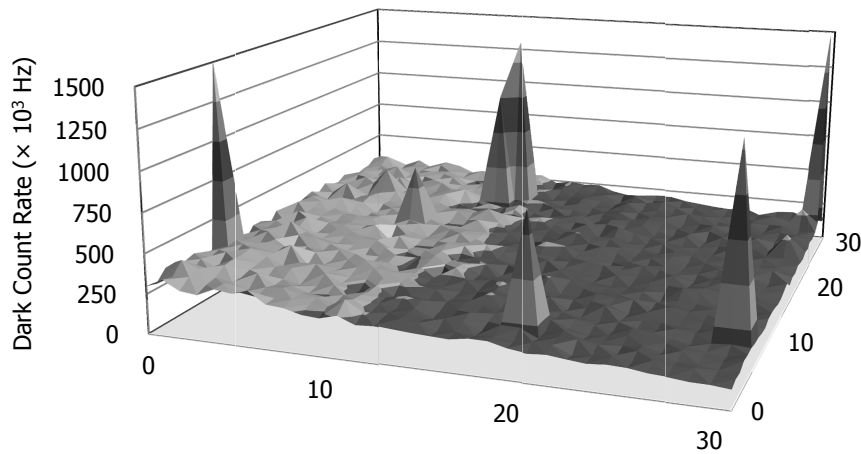


Figure 14. Distribution of the dark count rate across the 32×32 pixel array in the conditions of $V_e = 1.5$ V, $T = 242$ K

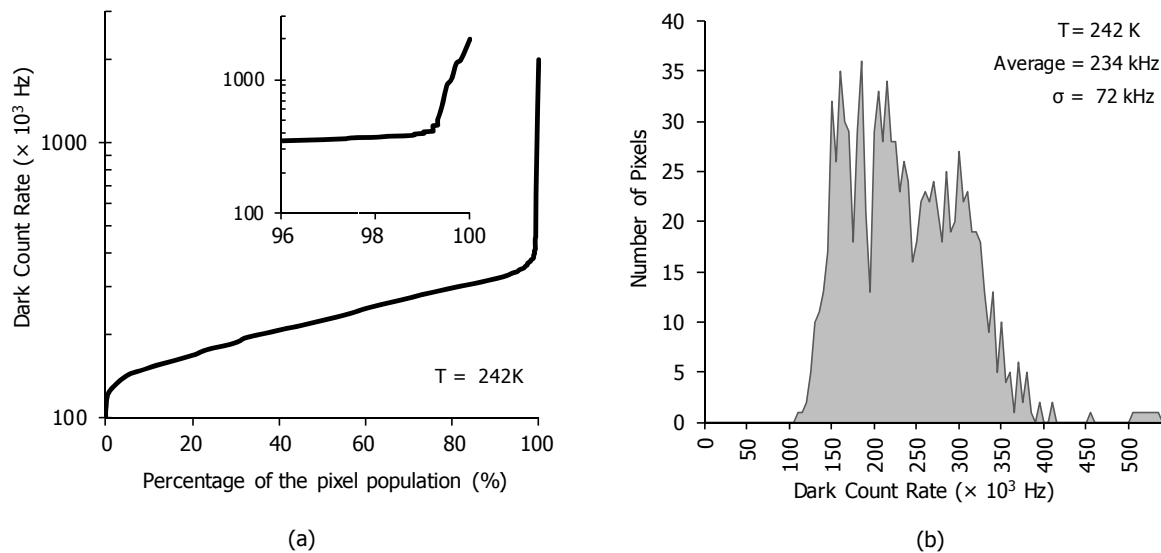


Figure 15. Statistical analysis of the dark count rate. (a) The cumulative distribution as a function of the percentage of the population. (b) The distribution as a function of the dark count rate.

4.4 Photon detection probability at 1.55 μm

The photon detection probability (PDP) is a parameter for the sensitivity response on Geiger-mode devices which is composed of the quantum efficiency (QE) and avalanche triggering probability. In this term, we exclude the geometrical fill factor of the SPAD sensor from the calculation. When the fill-factor is included in the sensitivity calculation, the term should be called photon detection efficiency (PDE), which is also generally used in SPAD studies. Since the InGaAs SPAD has the SAM structure as explained in section 1.2, the quantum efficiency is mainly defined by the InGaAs absorption layer, and the avalanche probability is defined by the electrical field strength within the multiplication layer where holes from the absorption layer contribute as seeds for triggering impact ionization.

The photon detection probability measurements were performed in the following way. An LED with peak emission wavelength at 1.55 μm was operated in DC, and the sensor plane was uniformly illuminated. As the same way of the DCR measurements, the number of pulses of each pixel was collected under both illuminated state and dark state. The number of incoming photons on the individual active area was estimated by the photocurrent of an InGaAs photodiode located in parallel beside the image sensor. The afterpulse of each pixel was also measured at the same time; therefore after all measurements were performed, the fraction of afterpulse was subtracted from the measured PDP values. In these measurements, the hold-off duration was set as 200 ns. So the values of the afterpulse probability were distributed in the range of 20 – 40%. This difference could be explained by the tilted distribution of the V_b . Figure 16 shows the PDP mapping excluding afterpulse probability, and the values were 10 – 12%.

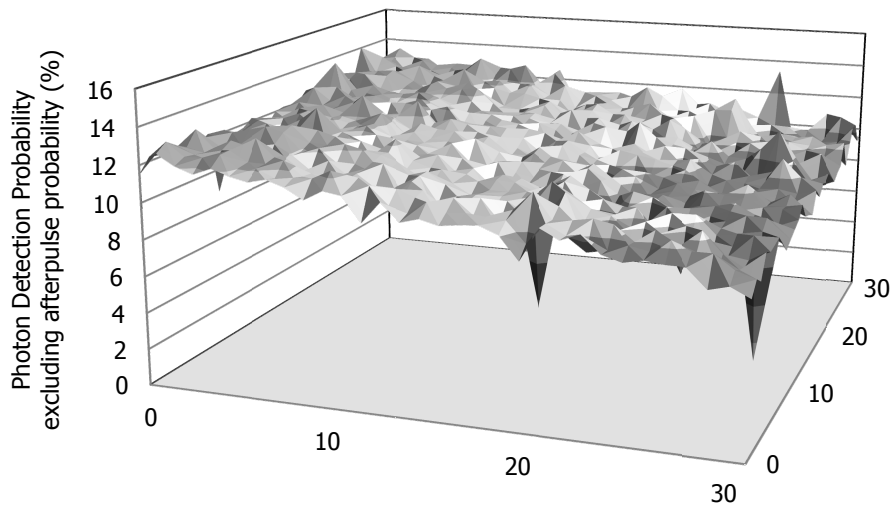


Figure 16. Distribution of the photon detection probability across the 32×32 pixel array in the conditions of $V_e = 1.5$ V, $T = 242$ K by illuminating an LED ($\lambda = 1.55 \mu\text{m}$) in DC.

4.5 Timing jitter evaluation by the in-pixel time-to-digital converters

In order to confirm the temporal resolution including both the InGaAs SPAD and the TDC, the timing jitter study was performed by utilizing the in-pixel TDCs. Figure 17 shows the brief description of the experimental setup. A short pulse laser ($\lambda = 1.537 \mu\text{m}$, pulse width = 46 ps) was used. To concentrate the short laser pulses within a few μm diameter, a light collection optical system with an objective lens ($\times 100$, Mitsutoyo) was used. The laser pulses were attenuated to have very weak light condition. The trigger for firing the laser head was adjusted via the delay generator.

Figure 18(a) shows the integrated image of 10000 frames when the laser pulses were concentrated at $(X, Y) = (14, 13)$. The histogram of the time measurement on the illuminated pixel is shown in Figure 18(b). The histogram distribution was fitted by Gaussian function to calculate the full-width half maximum (FWHM) values. Figure 19 shows the plot of the FWHM values as a function of the excess bias V_e . In accordance with the V_e , the decrease of the FWHM values was observed. For confirming the validity for the in-pixel TDC based measurements, additional measurements were performed by employing a fast oscilloscope (WaveRunner 8254M, Teledyne LeCroy) and the signal line which could monitor the AQC output directly. The FWHM values on the oscilloscope were calculated by the histogram function on the scope. The results are also shown in Figure 19. The value obtained by the oscilloscope at $V_e = 1.6$ V was approximately 260 ps. On the other hand, the FWHM value obtained by the TDC was approximately 453 ps. Assuming

the statistical fluctuation of the TDC is approximately 380 ps (1.2 LSBs), the estimated timing jitter of the SPAD can be calculated by the following simple calculation (2).

$$\Delta t_{SPAD} = \sqrt{\Delta t_{System}^2 - \Delta t_{TDC}^2 - \Delta t_{Laser}^2} = \sqrt{453^2 - 380^2 - 46^2} = 242 \quad (2)$$

The calculation result is well matched with the jitter evaluation by the oscilloscope. Therefore we can conclude that the timing jitter measurements by the in-pixel TDCs are valid. Table 1 summarizes the performance of the InGaAs SPAD image sensor obtained in this work.

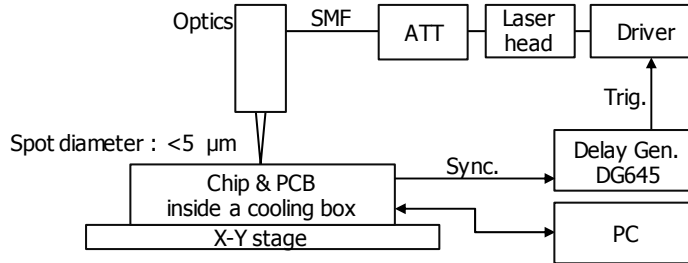


Figure 17. Instruments setup for the timing jitter measurements. The SPAD chip was installed within a cooler box.

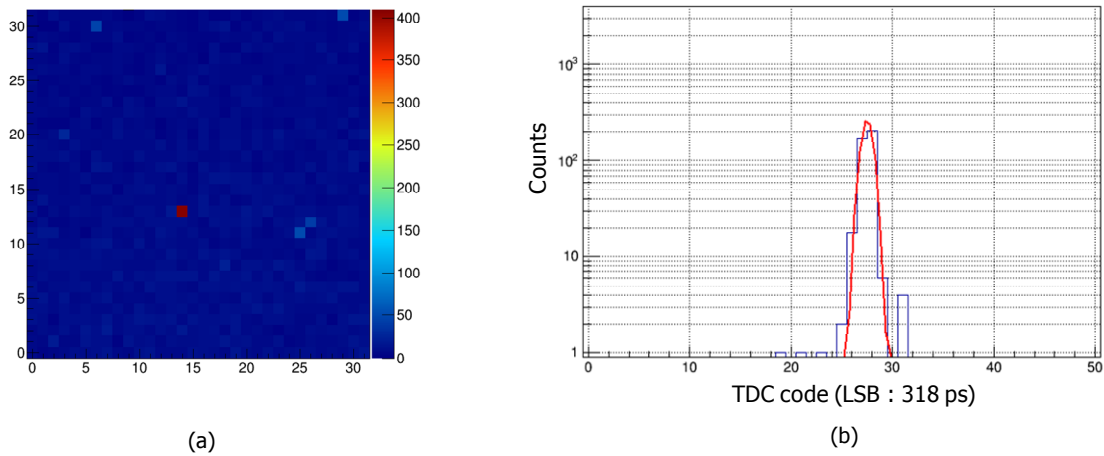


Figure 18. Timing jitter measurements in the conditions of $V_e = 1.6 \text{ V}$, $T = 255 \text{ K}$ at $(X, Y) = (14, 13)$. (a) Two-dimensional map when illuminating the laser. (b) Histogram of the output of the TDC and a Gaussian curve fit.

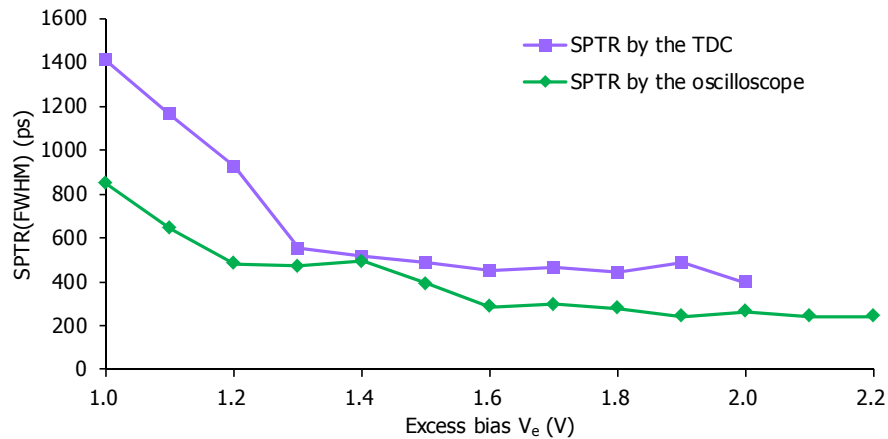


Figure 19. Comparison of Single Photon Timing Resolution (SPTR) as a function of the excess bias V_e generated by the in-pixel TDC and the oscilloscope

Table 1. Performance summary of this work

Part	Parameter	Condition	Min.	Typ.	Max.	Unit
Pixel	Photon detection probability	242 K, $V_e = 1.5$ V		10		%
	Dark count rate ¹	242 K, $V_e = 1.5$ V		234		kHz
	Spectral response	300 K, $M=1$	0.8	1.55	1.69	μm
	Afterpulse probability	251 K	5.6		92	%
	Temporal resolution	255 K	241		800	ps
ASIC	Adjustable hold-off duration	-	10		800	ns
	Global clock frequency	250 K	110		315	MHz
	Resolution of the TDC	250 K	200	318	600	ps
	Dynamic power dissipation of a pixel circuit	250 K		200		μW

¹ The diameter of the active area is $12 \mu\text{m}$

5. CONCLUSIONS

The back-illuminated InGaAs SPAD array with the in-pixel TDC for eye-safe Flash LIDAR have been fabricated and characterized. The frontend circuit has the active-quenching and recharge function to control the Geiger-mode operation of the InGaAs SPAD certainly by the adjustable quenching duration. As the duration is set for a longer period, the afterpulse probability was clearly decreased down to a few tens %. Breakdown voltage, DCR, and PDP mapping across the entire 32×32 2D array were characterized. The breakdown voltage exhibited excellent smooth distribution and its deviation came within a range of 292 mV (FWHM). This fact demonstrated that the electrical field was sustained uniformly across the entire $100 \mu\text{m}$ pitch 2D arrays. Although several pixels had large DCR values, 99% of 32×32 pixels showed fewer than 350 kHz at 245K. The PDP and the afterpulse probability of each pixel were characterized by a $1.55 \mu\text{m}$ LED, and the PDP distribution was 10 – 12% after subtracting the afterpulse probability. The intrinsic timing jitter of a SPAD was 260 ps at $V_e = 1.6$ V. The timing resolution of the one pixel system including the SPAD and the TDC was examined and the resolution was approximately 453 ps in which the contribution of the TDC was 318 ps. As the prototype has been characterized, we will perform practical imaging experiments and improve the performance of the InGaAs SPAD arrays and the ASICs in the near future.

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