Nanoelectronics - A Military Perspective

Gerald M. Borsuk

Electronics Science and Technology Division
Naval Research Laboratory
Washington, DC

abstract

The opportunity afforded by nanoscience and technology offers a broadening of scope in electronics technologies and creates the foundation for the Nanoelectronics Era. Superior electronics is a major "force-multiplier" for military systems. It is anticipated that nanoelectronics will augment the power of this multiplier. This paper explores the scientific and technological trends that will produce nanoelectronics and gives a few examples of the military applications of this emerging technology.

1. Introduction

Nanoelectronics is an emerging new class of electronic devices that contain features of nanometer size dimension and exhibit new physical phenomena with the potential to extend digital technology beyond the current ultra large-scale integration (ULSI) horizon. It is an area of increasing research emphasis within the private and government research sectors that has important commercial and military implications for the future. For the commercial sector, continued improvements and new capabilities in information and highly integrated electronic technologies that improve the quality of life and our living standard can be expected. For the military sector, new capabilities in electronic systems and sensors for real-time battlefield intelligence, situational awareness, command and control, surveillance, and smart weapons can be envisioned. Although the path to travel is reasonably clear, there are significant technical challenges that must be overcome in the next ten to fifteen years to enable a successful transition from the present age of "microelectronics" to the new age of "nano-electronics". Some key technical issues and their potential impact on military capabilities are presented.

Nanostructure Science, Metrology, and Technology, Martin C. Peckerar, Michael T. Postek, Jr., Editors, Proceedings of SPIE Vol. 4608 (2002) © 2002 SPIE · 0277-786X/02/$15.00

2. **Discussion**

The attributes of silicon MOS device scaling, first articulated by Dennard, et.al.(1), have propelled the information and microelectronics technology revolutions of the past 30 years. Scaling to smaller dimensions has led directly to faster electronics that consume ever-lower power, are capable of greater data processing, and have ever more complex information and sensor processing capabilities. The commonly referred to Moore's Law (2) is a prediction based upon MOS device scaling through improvements in semiconductor manufacturing technologies, that the number of active devices on a silicon Very Large Scale Integrated Circuit (VLSI) die will double about every 18 months. The consequence is ever increasing performance benefits (higher speed and lower power dissipation per device), as Moore's Law has been uncanny in its accurate prediction of performance and device density trends in silicon MOS VLSI over this period of time.

Given continued improvements in semiconductor manufacturing technology, Moore's Law will likely remain valid for the next 8 to 10 years. However, even within this time period, for device feature sizes on the order of 50 nanometers or less, significant barriers most be overcome. They include the transition to a new generation of lithography tools not based upon conventional projection optical methods and significant economic barriers attributed to the multiple billion dollar cost of outfitting and operating large scale semiconductor fabrication facilities. Also, in the feature size range below 50 nanometers to about 30 nanometers, conventional silicon MOS scaling improvements in speed and power dissipation diverge from what is expected from the conventional scaling rules. Quantum effects more clearly affect device operation and performance in this regime. At this point, the transition to the nanoelectronics regime will begin. In the dimensional range below 10 nanometers (the size of small molecules), quantum effects dominate electronic behavior at room temperature and other physical and electronic phenomena appear. At this scale, the minimum size for electronic device and circuit functionality will have been reached. Figure 1 presents key electronic circuit functions (DRAM and processors) as function of time and critical electronic parameters extracted from the International Technology Road for Semiconductors 2000 Edition. This chart shows the transition to the Nanoelectronics Era occurring in the 2009-2012 time period.

Year 1st ship	1995	1997	1999	2001	2003	2005	2009	2012
DRAM (bits/chip)	64M	256M	1G	2G	4G	16G	64G	256G
DRAM chip size (cm2)	1.9	2.8	4.0	4.5	5.6	7.9	11.2	15.8
mP transistors/cm2	2.0M	3.7M	6.2M	10M	18M	39M	84M	180M
mP chip size (cm2)	2.5	3.0	3.4	3.9	4.3	5.2	6.2	7.5
Lithography (nm)	350	250	180	130	100	90	60	35
Oxide thickness (nm)	7-12	4-5	3-4	2.4-3.2	2-3	1.5-2	<1.5	<1.0
Supply Voltage (V)	3.3	1.8-2.5	1.5-1.8	1.2-1.5	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6
Clock (MHz)	300	750	1400	2100	3000	4000	-	-

Figure 1.Key integrated circuit parameter trends past,present,and future.

The transition to the nanoelectronics circuit regime will likely involve three distinct device generations. The first generation of nanoelectronic devices and circuits that will evolve over the next ten years will be based upon the genetic cousins of well understood transistors of today but in bandgap engineered materials such as those involving the 6.1 Angstrom family of III-V semiconductors, SiGe, magneto-electronic, and bio-electronic materials. A second generation of nanoelectronic circuits that will evolve in the ten to twenty year time frame may involve hybrid forms of the single/few electron transistor with spin polarization properties and carbon nanotube electromechanically self assembled quantum effect devices. The next and likely final generation of nanoelectronic devices and circuits that will evolve in the twenty to forty year time frame will likely be based on the complex interactions between electronic states of mater, the quantum coherence between electron states in semiconductors and metals, and wave function electronic interactions manifested in circuits as so-called Qubits. In all of these stages of development and utilization, key

challenges to over come will include economical device and circuit fabrication, the architecture of the nanoelectronic circuit including novel signal and data processing algorithms, the interface methods and mechanisms between the nanoelectronic circuit and the micro/macro-circuit, and the integration of such circuits into functional sensors and networks.

The research offices of the military services (ONR, ARO, and AFOSR) and defense agencies (DARPA) have invested in both their in-house laboratories (NRL, ARL, and AFRL) and the private sector (academia and industrial research laboratories) in all the important pacing areas of research necessary to improve our knowledge base in nanoelectronics. These R&D areas include device physics research, materials research, nanofabrication, and architecture research. In the area of device physics research has focused upon quantum-effect devices, single-electron devices, and magneto-electronic and nano-magnetic devices. A 60 nm InAs HEMT is shown in Figure 2 that has extremely low power

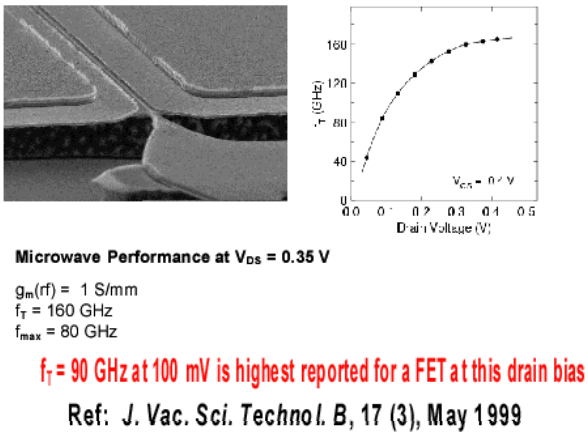


Figure 2. A 60 nanometer gate width very high speed InAs HEMT device with very low drain voltage.

consumption and very high speed (3). It is possible to use this device with a resonant inter-band tunneling diode in logic circuits that operate with >50 GHz clock rates at medium scale integration levels of complexity (1,000-10,000 logic elements). This is particularly attractive for applications such as communicastions and data fusion in autonomous stand-alone sensors.

The military has considerable need for radiation hard, non-volatile storage. Nanostructures that exhibited the giant magneto resistance (GMR effect) are potential memory element candidates and have formed the basis for a new class of nanometer scale high-density non-volatile memory. A test structure of a GMR vertical cylindrical device is shown in Figure 3(4).

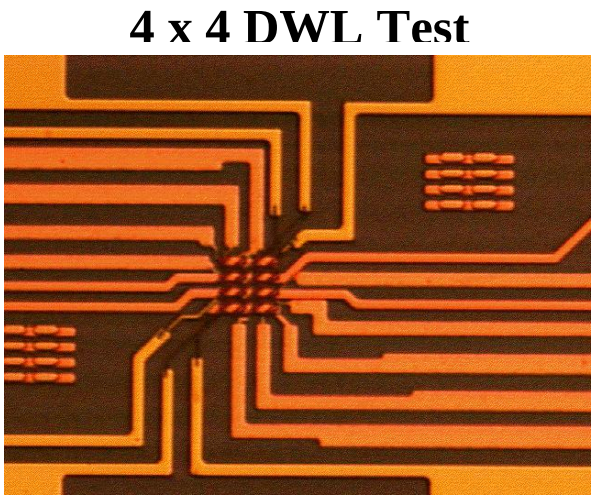
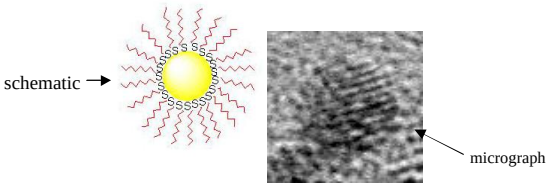
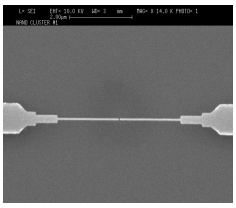


Figure 3. A GMR Vertical Cylindrical Non-Volatile Memory Test Array.

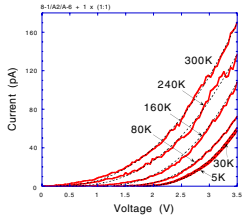
Nanometer sized structures demonstrate unique physical properties based on quantum mechanical phenomena. These phenomena do not occur in the "macroscopic" size regime. They can be capitalized upon to yield new electronic and sensor functionality. Nanostructures synthesized with total diameter of about 3 nanometers have been self-assembled onto pre-patterned substrates that show a strong non-linear current-voltage relationship due to Coulomb blockade as shown in Figure 4 (5). This work is significant because it shows this important effect at close to room temperature. The demonstration of a controlled solid-state Qubit with a relatively long phase memory of 3.6 micro-seconds detected in the spin of a nitrogen vacancy in diamond at very low temperature is a recent scientific result

A. The gold nanocluster





B. Self-assembly onto pre-patterned substrates



C. Strongly nonlinear I-V characteristics due to Coulomb blockade

Figure 4: Gold nanoclusters exhibit Coulomb blockade at near room temperature

that builds the knowledge base for a better understanding of the possibilities of achieving quantum computing (6).

New pattern formation methods that require direct physical manipulation of single atoms and molecules are crucial to economical fabrication of nanometer sized devices and circuits. Throughput with high yield will eventually determine the way ahead. Several approaches to nanoelectronic pattern formation include scanned probe lithography and directed self-assembly. An example of a scanned probed lithography approach to nanometer-scale lithography involves single-wall carbon nanotubes attached to AFM tips as shown in Figure 5 (7,8).

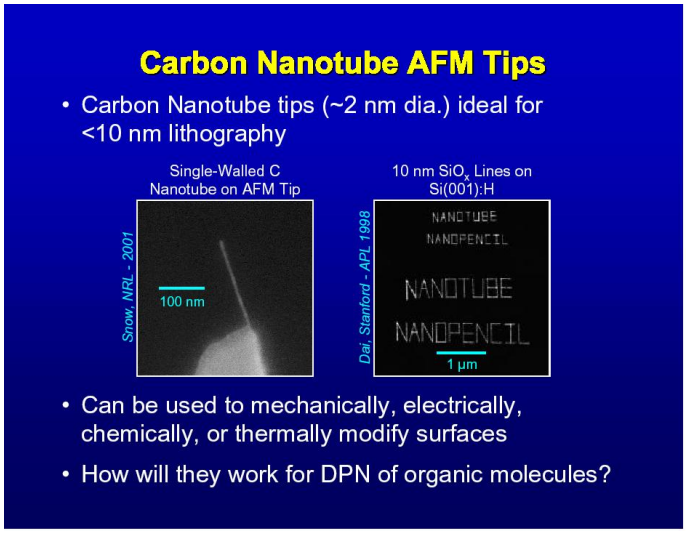


Figure 5. Carbon Nanotubes used as a lithography tool

Electronics on the molecular scale attempts to solve the problem of nanometer scale device fabrication by using chemical assembly to form atomically precise molecules with tailored electronic properties. However, challenges remain on how to bridge the size gap between molecular structures (<10 nanometers) and the minimum feature size of lithographically defined interconnections (~100 nanometers). One approach to bridge this gap is to use directed self-assembly to build a mesoscale bridge between the two size domains. Such molecular robes and anchors are shown schematically in Figure 6 (8).

In summary, scientific research conducted in government laboratories and the private sector is increasing our knowledge across a broad spectrum of materials, device, and architecture disciplines pointing the way to the new regime of nanoelectronics.

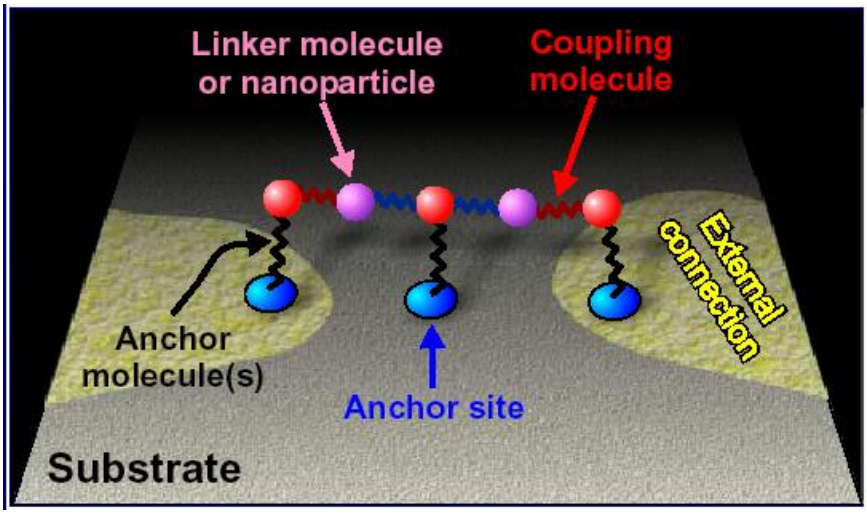


Figure 6. Conceptual view of molecular robes and anchors for bridging the gap between the nanometer and mesoscopic size regimes.

3. Military Applications

A key attribute of modern warfare now and in the future is the use of advanced electronics and information technologies. The ability to process sensor and other information data at very high speed, analyze it, distribute it, and act upon it has given the US military unparalleled technological superiority in the battlespace. To maintain this leadership and avoid technological surprise in the battlespace, it is necessary that the DoD continue to push forward the research and development of advanced electronics so that as a nation we have first access to resulting technologies and the opportunity to apply first the capabilities they can enable in our systems. To decrease the time needed to insert these technologies as they appear in the industrial sector and to improve affordablity much emphasis has been placed upon the use of commercial off the shelf parts in emerging military systems. This emphasis has been modulated by the need to maintain military ruggedness and in some cases to give superior performance. It is possible that some very superior military capapbablities may be provided in the future by nanoelectronic components that do not meet commercial economic constraints for large scale production.

A few examples demonstrate the future need and opportunities afforded by the coming Nanoelectronics Era. Military platform protection against a threat can be

viewed in the abstract as speed of detection, rate of processing detected information, and response. These attributes can be presented in a formulation that relates system clock speed requirements to speed of engagement, volume of the engagement field, and algorithm complexity as shown in Figure 7 (9):

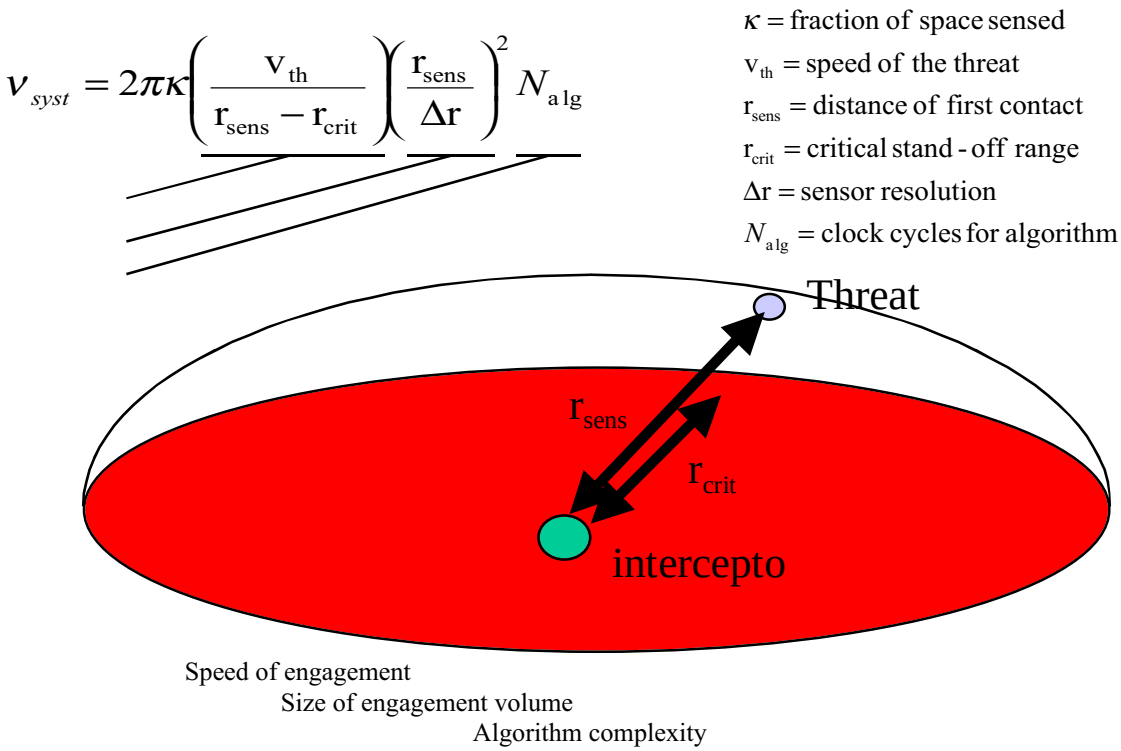


Figure 7. System clock speed requirements in terms of threat engagement speed, search and track volume, and signal processing algorithm complexity.

Projected capabilities and parameters indicate that over the next 10 to 15 years, a factor >10 increase over current state-of-the-art processing speeds will be required to protect platforms from emerging threats.

Processors base upon high speed nanoelectronics is a candidate to fill this performance gap. Other areas of application of the capabilities that nanoelectronics promise include Unmanned Aerial Vehicles (UAVs) and bio-chemical sensors. Future UAVs will demand very high speed processing of complex sensor signals requiring high processing power with low power consumption and small size. Based on the figure of merit TFLOPS/(power x volume) (where TFLOPS is a trillion floating point operations per second), values on the order of 1 TFLOPS per (watt x cm^3) may be necessary in the 2015 time frame to perform real time image processing and threat

recognition on-board micro UAVs. Bio-chemical sensors will benefit from the integration of nanometer sized sensing elements coupled with electronics that implements detection algorithms and information distribution in very small and economical produced packages. Over the next ten years, the electronics to do this function will be those afforded by mesoscale ULSI while in the Nanoelectronics Era sensors will be fabricated with integrated nanometer feature size integrated circuits with very high speed processing capability affording a wide range of protection against biological and chemical threats.

Nanoelectronics is today a scientific endeavor with high research opportunity that will contribute to military capabilities in the future.

4. **A Strategy, Summary, and Conclusions**

The DoD has overarching electronic and sensor needs that correlate extremely well with the major forefronts of physical and biological nanoscale science and technology. Continued support over the long term, emphasizing multi-disciplinary research, is necessary to create new knowledge in the areas of nanoscience and nanotechnology that are leading to the nanoelectronics era. This support will also help ensure the availability of nanoelectronics to our military of the future. Opportunities to spin off scientific advances to technological development of significant military importance will exist through out the entire period as present ULSI electronics transitions to the nanoelectronics era. These opportunities should be seized as appropriate as the long term scientific base continues to be nurtured. Richard Feynman observed in the early 1960s that there was still plenty of room at the bottom. His vision is as true today as it was then and will be over the next forty years.

5. **Acknowledgment**

The author wishes to acknowledge the critical review and comments of Dr. Martin Peckerar, Dr. Christie Marrian, and Dr. Eric Snow all of the Naval Research Laboratory, Washington, DC.

6. **References**

1. R.H. Dennard, F.H. Gaenssem. H.-N. Yu, V.L. Rideout, E. Bassous, and A.R. LeBanc, "Design of ion-implanted MOSFETs with Very Small Physical Dimensions," IEEE Journal of Solid State Circuits, vol. SC 9, pp.256-268, October, 1974.

2. G.E. Moore, " Progress in Digital Integrated Circuits", in Technical Digest, 1975 International Electron Devices Conference, Dec.,1975, pp.11-13.

3. B. Boos, B.R. Bennett, W. Kruppa, D. Park,J. Mittereder, R. Bass, and M.E. Twigg, "Ohmic Contacts in AlSb/InAs High Electron Mobility Transistors for Low-Voltage Operation", J. Vac. Science Technology B,17(3), May/June, 1999, pp1022-1027.

4. Personal Communications, Gary Prinz, Sept., 2001

5. Mario Ancona, W. Kruppa,, R.W. Rendell, A.W. Snow, D. Park, and J.B. Boos, "Coulomb Blockade in Single-Layer Au Nanoclusters," Phys. Rev. B 64, 033408, 2001.

6.F.T. Charnock and Thomas Kennedy, "Combined optical and microwave approach for performing quantum spin operation on the nitrogen-vacancy center in diamond," Phys. Rev. B64, 041201, 2001.

7. SEM of C Nanotube AFM Tip, Personal Communications, Eric Snow, Sept., 2001

8. H. J. Dai, N. Franklin, J. Han, "Exploiting the Properties of Carbon Nanotubes for Nanolithography", Applied Physics Letters 73☹11), pp 1508-1510, September 14, 1998.

8. Personal Communications, Lloyd Whitman and John Russell, Sept, 2001

9. Personal Communications, Martin Peckerar, Sept, 2001