In the End It's the Bottom Line That Counts

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Introduction

Electronics has been the nation's largest and fastest growing manufacturing industry throughout the end of the last century. Semiconductors have fueled that growth, even with the downturn in the past two years. The US semiconductor industry now has the largest value-added of any US manufacturing sector, comprising almost 1 percent of US gross domestic product (GDP). In 2001 US-based firms accounted for approximately 52% of the $140-billion world semiconductor market, and the electronics industry employs more than 2 million Americans. This growth has been sustained through steady advancements in semiconductor manufacturing science and technology. These strategies have lead to increasingly cost effective advanced communications and information technologies.

The Roadmap

Growth in this dynamic industry is not assured unless it maintains the pace of advancement in the manufacturing technologies that control the rate at which future generations of electronic products emerge. Microlithography is one of the most essential of such technologies. The pace of the roadmap will continue unabated until equipment and materials, along with physics and economics limit continued decreases in feature sizes. Currently the semiconductor industry is focused on the availability of lithographic tools to maintain the roadmap. The industry is moving belo the 100nm node (gate printed image in resist of 65 nm), with several companies announcing the availability of 90nm production this year. Based on physics and the current tool design point (Rayleigh equation), the intersection between the roadmap and the minimum feature size capability at 193nm will be reached in 2004-5. The plan

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was to introduce 157nm lithography to maintain the roadmap. Over the past two years 193nm immersion lithography has been aggressively pursued as an alternative approach to 157nm and first generation development tools should be available within the next 18 months. The immersion liquid is water, and research has been started to find higher refractive index materials that would extend 193nm lithography even further into the future. However, the key to progress on smaller feature sizes will be the availability and cost of the mask and related infrastructure. Not just for 157nm and EUV but even for pushing the limits at 193nm.

There are at least two near term requirements to maintaining the roadmap: 1) ability to operate in manufacturing at the fundamental limits at193nm with available masks and 2) the economics of these solutions.

The Pace of Technology Introduction

In fact the history of the past twenty years serves as both enlightenment and warning. Each move to a shorter wavelength has taken longer than expected. In the case of 193nm, SEMATECH and the industry put together a focused program in 1994 with a goal of introduction of manufacturing tools at 193nm in production by 1999/2000. The fundamental tool designs remained constant with the prior (248nm) generation, ask blanks and materials for binary masks remained constant, resists needed significant work but could be screened initially using the 248nm tools in production. A full field tool existed at MITLL and several mini-steppers for development work were delivered by 1996. Major tool suppliers had orders from customers and were designing and building the first tools for shipment in 1998-9**. The result of this industry focused and financed effort: 193nm in limited production in manufacturing in 2002-3**. That is ten years after there were full-field tools, 6-7 years after ministeppers were established in multiple laboratories. In addition, the early part of the research/development cycle corresponded with a peak of profitability in semiconductors and equipment: 1995-8. This profitability allowed significant investment in the next generation lithography.

Funding Infrastructure Development

Mask development, mask writers, repair and inspection are essential elements of the lithographic system. Today, the mask industry is in a uniquely perilous situation. Whereas semiconductor manufacturers sell millions of chips and lithography tools are in hundreds per year, the mask equipment industry has total tool sales of 15-20 per year for mask writers and less than ten for mask repair. Thus the cost of development must be recovered over only a few tools. These tools are critical to the entire roadmap and semiconductor manufacturing. The mask industry, along with its equipment and materials suppliers lack the financial strength to meet the growing technical demands identified in the roadmap. Escalating R&D costs and small markets contribute to this deteriorating situation. Since the mid-nineties many semiconductor manufacturers have eliminated their captive mask shops, outsourcing their mask supply in the drive for lowered total cost for the masks This has resulted in significant consolidation. While these consolidations have improved the efficiency of mask making they also have had the effect of decreasing the total available market for the equipment infrastructure necessary to build next generation masks. Over the past three years there has been a significant reduction in the number of ASIC tapeouts driven in part by the downturn, in part by the rapidly escalating costs for advanced masks. This has resulted in excess capacity and, lowered tool sales and less R&D expenditure.

Low chip sales → low mask sales → excess capacity → low equipment sales→
Limited investment in future technology

Mask house consolidation-→ excess capacity → low equipment sales→
Limited investment in future technology

And for the mask makers lowered profits mean lowered investment in process integration, and yield learning.

Maintaining the ITRS roadmap for feature size using 193nm continues to be a significant challenge. As the industry uses 193nm for ever smaller feature sizes, more demand is being placed on the mask capability. In recent meetings discussion has centered on the possibility that as the mask features approach the wavelength of light additional polarization effects will be seen. Over the past year the advances towards 193i and difficulties with supply and integration of 157nm tools has placed the 157nm technology viability in doubt. An analysis of the 193nm timeline would lead to a projection for EUV in production sometime after 2010. Equipment suppliers are being asked to develop custom equipment well in advance of potential for multiple tool sales.

Support of the crosscutting technologies is essential to ensure a strong infrastructure capable of sustaining the pace of the semiconductor industry. Mask development, mask writers, repair and inspection are essential elements of this infrastructure. The cost of development is much higher than is affordable. This industry, along with its equipment and materials suppliers lack the financial strength required to meet the growing technical demands identified in the roadmap. Today, mask availability and the escalating costs for advanced masks is one of the biggest risks to the future of the industry. In order to reduce this risk significant resources need to be applied to overcome the barriers to high yield advanced mask production. Or breakthrough approaches, new technologies must be found. The current escalating costs of masks driven primarily by the cost of writing the mask is unaffordable. New models and better partnership between customers and suppliers is needed to address this significant problem.

Capability to meet the demands of the roadmap will require sustained investments by both the public and private sectors and the continued innovation of academia. Timely access to leading edge capability is critical to maintain the pace of the roadmap.

Optics Forever?

The goal has not changed over the past 20 years: extend optical lithography as far as possible, and then farther. It is possible that the use of immersion lenses with liquids of higher refractive index will extend optical lithography, and 193nm, well below 45nm. The process window has been increased by the application of optical enhancements such as off-axis illumination systems, optical proximity correction on masks and advanced resists. One can expect continued focus in these areas. These optical enhancements increase the process window but also significantly increase the difficulty for mask making, and even design, as feature sizes move below 100nm. Increased difficulty and complexity mean exponentially higher costs at these dimensions. So we have a situation where the cost of lithography equipment is escalating and the costs of masks are increasing even faster.

Affordable Lithography ?

The fundamental driving force has been the continued growth in the level of integration, speed and features while maintaining the average cost per chip, with ever decreasing cost per bit. It's the cost per wafer that counts. It starts with consumer electronics, the volume market, and works backwards. What is the affordable price for a semiconductor chip? And what profit margin does the semiconductor manufacturer need to be successful? In the volume market there is not a lot of potential to increase the price of chips. Thus the affordable cost for processing a wafer can be calculated. For 200mm SEMATECH calculated that to be between1200-1800 dollars, for 300 approximately $3000. The rest is arithmetic.

Most tools can process a 300mm wafer in approximately the same time as a200 wafer. However smaller feature sizes, tighter process controls, thinner materials, and tighter defect controls do not lead to less expensive tools or processes for any level. Increased wafer sizes result in a productivity/cost advantage because the cost/area to produce chips is less.

In the keynote presentation at the EUV meeting in 2002 Peter Silverman spoke about the productivity requirements for a lithography tool to be used in manufacturing. He had a simple algorithm:

The thruput of the tool must be greater than 6X the tool cost in millions of dollars or the tool "will not be used in manufacturing".

Lithography tools today meet or exceed that target. He also said the mask costs should not exceed the costs of a 248nm mask at the 180nm node. Even today we greatly exceed that target for critical level masks. We have extended the life of the lithography tool generations by increasing the complexity of the mask. The next generation tools were not mature enough, or even available when needed. By the old paradigms we needed 248 for 250 nm, 193 at 200nm and 157 for 150nm. So now we are at 193 for 90, 65, 193i for 45…32nm. Using a 193nm tool for these generations meets the Silverman algorithm, but not the mask. With current cost/throughput estimates for the next generation tools, they will also greatly exceed that target. Current aggressive cost and thruput numbers for an EUV tool would put the ratio at 0.33, and maskless tools at a cost projected cost of $25M and 5 wafers per hour are perhaps useful in development, but with a ratio of 0.2 are too expensive for manufacturing.

Maskless?

Studies on maskless approaches have generally looked at the projected mask costs at a given node and then calculated the number of wafers for which maskless

lithography would represent a significantly lower cost. For example at the 65nm node a mask set is expected to cost $3.5 M. If you need less than 500 wafers per mask it is cheaper to use a maskless tool. However if you do an actual cost calculation you find that both approaches greatly exceed the affordable processing costs per wafer. For a product run of 1000 wafers just the mask cost per wafer($3500) would exceed the total target cost. If you assume a maskless tool cost of $25M, 5 wafers per hour, 50% utilization, the total wafers processed in one year would be less than 25K. With 5year depreciation, the tool depreciation cost per wafer would be $200. The tool depreciation costs to process the 16 critical layers would be $3200.

To stay on the roadmap requires:

Litho tools and masks that meet the Silverman algorith

Or a maskless tool which meets a “modified” algorithm: 5x?

Or new breakthrough technologies, or a new model??

Summary

The industry is rapidly approaching the point where the economics behind the design and production of semiconductor chips will be as visible as the physics of semiconductors has been until now. The growth in the electronics industry has been fueled by technology that is lighter, faster, cheaper. To continue on that path we must find ways to make devices smaller, faster and cheaper. We need some of the emerging technologies to provide breakthroughs, and new paradigm that allow the industry to continue its fabulous success.