Block Copolymer Directed Self-Assembly Enables Sublithographic Patterning for Device Fabrication

H.-S. Philip Wong[1], Chris Bencher[2], He Yi[1], Xin-Yu Bao[1,†], Li-Wen Chang[1,#]

[1] *Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA*

[2] *Applied Materials, Inc., 3050 Bowers Avenue, Santa Clara, CA 95054, USA*

[†] *Present affiliation: Applied Materials, Inc., 3050 Bowers Avenue, Santa Clara, CA 95054, USA*

[#] *Present affiliation: Xilinx Inc., 2100 Logic Drive, San Jose, CA 95124, USA*

Abstract

The use of block copolymer self-assembly for device fabrication in the semiconductor industry has been envisioned for over a decade. Early works by the groups of Hawker, Russell, and Nealey [1-2] have shown a high degree of dimensional control of the self-assembled features over large areas with high degree of ordering. The exquisite dimensional control at nanometer-scale feature sizes is one of the most attractive properties of block copolymer self-assembly. At the same time, device and circuit fabrication for the semiconductor industry requires accurate placement of desired features at irregular positions on the chip. The need to coax the self-assembled features into circuit layout friendly location is a roadblock for introducing self-assembly into semiconductor manufacturing. Directed self-assembly (DSA) and the use of topography to direct the self-assembly (graphoepitaxy) have shown great promise in solving the placement problem [3-4]. In this paper, we review recent progress in using block copolymer directed self-assembly for patterning sub-20 nm contact holes for practical circuits.

Recognizing that typical circuit layouts do *not* require long range order, we adopt a lithography sub-division approach akin to double-patterning and spacer patterning. Guiding topographical templates with sizes of the order of the natural pitch of the block copolymer can effectively guide the placement of block copolymer features at arbitrary locations irrespective of the natural (often hexagonal for cylindrical domains) arrangements of the block copolymer [5] (Fig. 1). This is possible because the forces from the lateral confinement from sidewall of the small topographical template are strong. Using small topographical templates, contact hole patterns that are often used in circuit layouts can be placed at arbitrary location by first patterning a coarse guiding template using conventional lithography [5-6] (Fig. 2). This procedure is akin to double-patterning and spacer patterning where a coarse lithographic pattern is used to generate a higher resolution feature at a location determined by the coarse lithographic pattern. The size and registration of the features are determined by parameters of the template as well as the block copolymer itself. Preliminary analysis of the size and positional accuracy of small template DSA shows great promise [6] (Fig. 3).

Alternative Lithographic Technologies IV, edited by William M. Tong, Douglas J. Resnick, Proc. of SPIE
Vol. 8323, 832303 · © 2012 SPIE · CCC code: 0277-786X/12/$18 · doi: 10.1117/12.918312

To illustrate the use of this small template DSA approach, we use 193 nm immersion lithography to print the templates for 22-nm node SRAM cells reported by IBM [7]. The contact for the polysilicon-to-diffusion cross-over of the SRAM cell is implemented by a two-hole contact pattern (Fig. 2c) instead of an elliptical contact in the original design (Fig. 4). Well-formed contact hole patterns with good positional accuracy are obtained (Fig. 5) using only one lithography step followed by block copolymer DSA.

Pattern transfer of the block copolymer soft mask into device layers is necessary for device fabrication. Using conventional reactive ion etching, DSA contact hole patterns are transferred to dielectric layers and subsequently filled with metals that make electrical contact to the devices [8] (Fig. 6). Transistors and simple circuits such as inverters have been demonstrated using block copolymer DSA for contact hole patterning [8] (Fig. 7). The contact holes for more complex random logic circuits patterned by this small template DSA approach has also been demonstrated for selected standard cells in an open-source standard cell library adapted for 22-nm node CMOS [9].

One of the main concerns for the commercialization of directed self-assembly (DSA) for semiconductor manufacturing is defectivity. A common application for this small template approach is to form a single hole for each coarse template (Fig. 2a) (hole-in-hole). The missing via defectivity rate using this DSA hole-shrink technique has recently been reported by others to be less than 1-per-25-million vias [10]. This result reinforces the commercializability of this patterning technique.

Acknowledgement

This work is supported in part by the NSF (CMMI 1029452) and Global Research Collaboration (GRC) of the Semiconductor Research Corporation (SRC).

Supplement

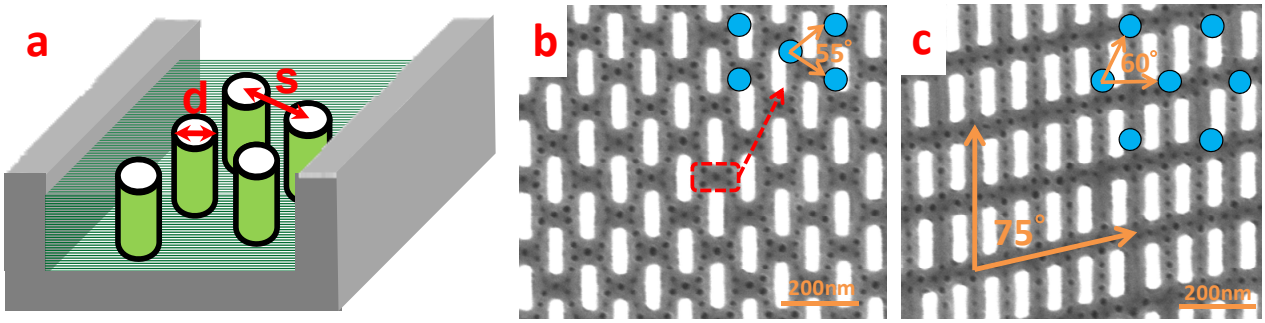

Fig. 1. (a) Graphoepitaxy with self-assembled cylinders aligned in the trench center. d represents the diameter of the cylinder and s represents the nearest center to center distance. (b) – (c) Self-assembled holes on pre-patterned templates with dimensional scales close to its nature size / pitch. The physical confinement forces the self-assembly to rearrange according to the array of the templates thus breaking the inherent hexagonal closed pack structure. Inset of (b) shows the included angle between two neighboring holes is 55°. Inset of (c) shows the hexagonal closed pack with an included angle of 60° while the templates in (c) drives the angle between neighboring holes to 75°. After Chang *et al*. [5].

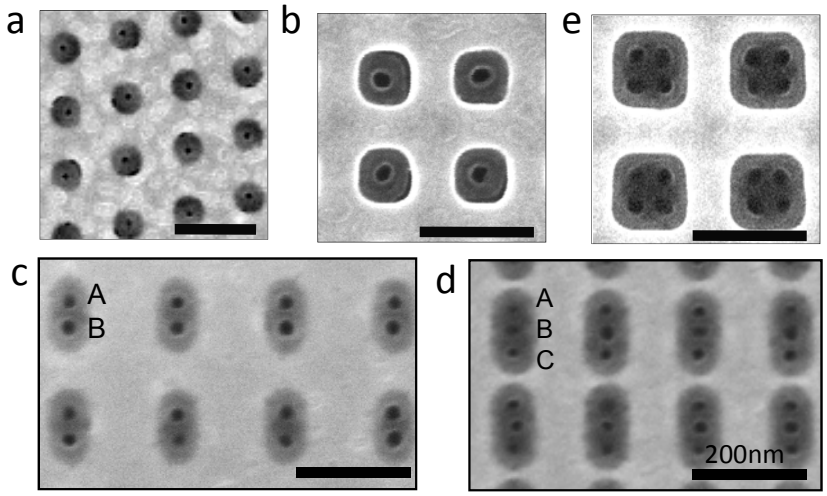

Fig. 2. SEM images of DSA patterns confined by small templates. Templates are patterned using conventional optical lithography and etched into 50 nm depths. Single hole in (a) 75 nm and (b) 92 nm square templates. (c) 4-hole square lattice patterns in 126 nm square templates. (d) 2-hole patterns in 60 nm × 110 nm rectangle templates. (e) 3-hole pattern in 70 nm ×145 nm rectangle templates. Scale bar 200 nm. After Bao *et al*. [6].

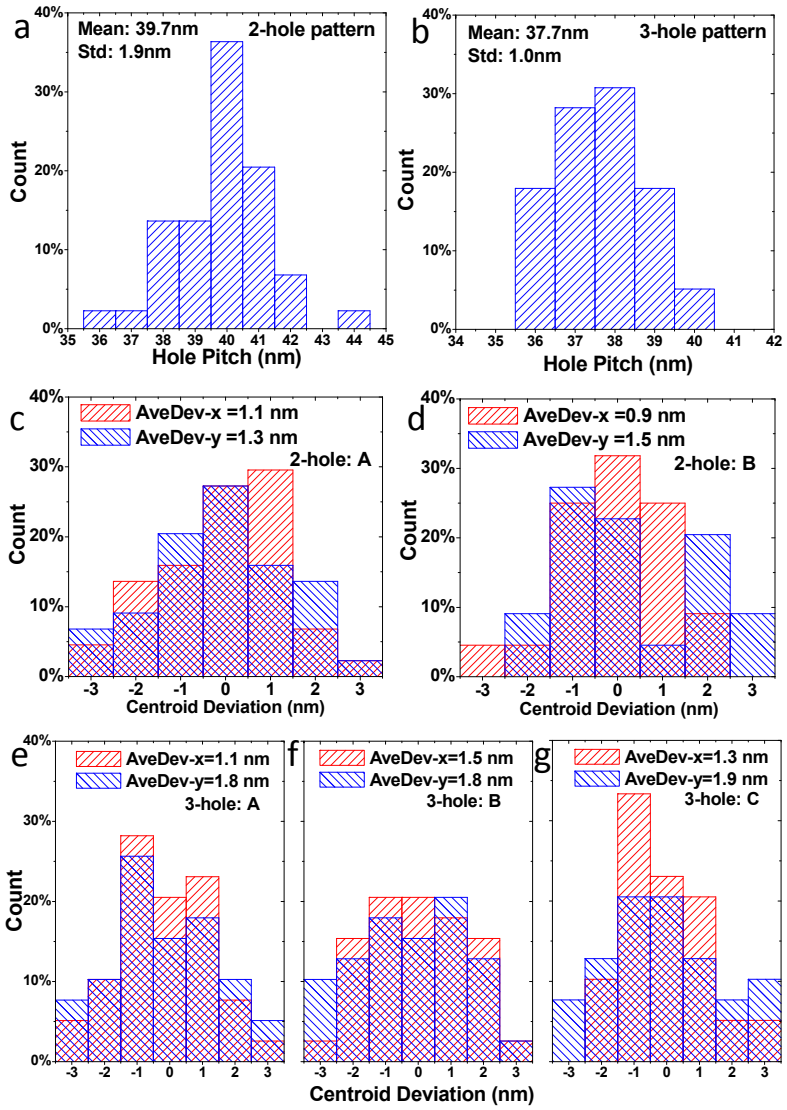

Fig. 3. The pitch analysis for (a) two-hole pattern in Fig. 2d and (b) three-hole pattern in Fig. 2e. (c) and (d) Overlay accuracy of two-hole pattern. The average absolute deviation (AveDev) in x and y direction is 1.1 nm and 1.3 nm (upper row hole A), 0.9 nm and 1.5 nm (lower row hole B), respectively. Overlay accuracy of three-hole pattern. (e) Upper hole A. (f) Middle hole B. (g) Lower hole C. The AveDev for all the DSA patterns is less than 2 nm, indicating a good position registration accuracy and repeatability. After Bao *et al*. [6].

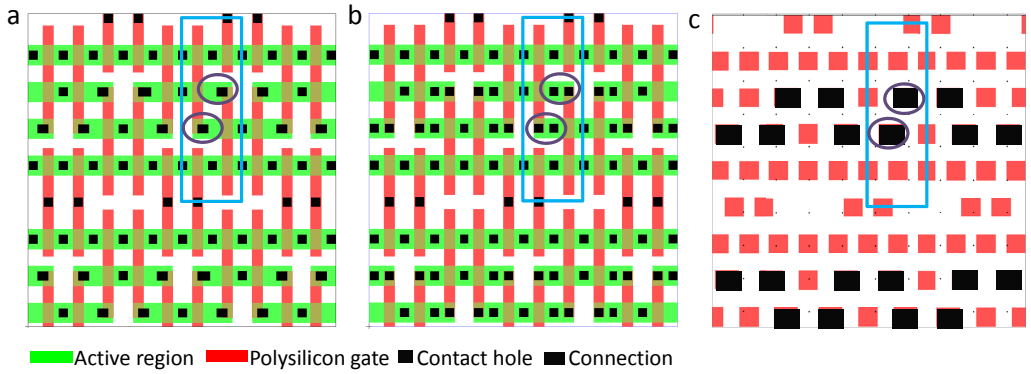

Fig. 4. (a) Contact hole layout derived directly from the IBM 22-nm 6T-SRAM [7]. A unit cell is outlined by a blue rectangle (dimension 180 × 554 nm^2). (b) Modified layout by replacing the rectangular connections with hole-pairs (highlighted by purple ellipses). One hole contacts the active region and the other hole contacts the polysilicon gate. (c) Immersion 193 nm optical lithography mask design for guiding templates of SRAM contact holes. Black rectangles are designed for the two-hole patterns as connections between the polysilicon gate and the active diffusions. After Bao *et al*. [6].

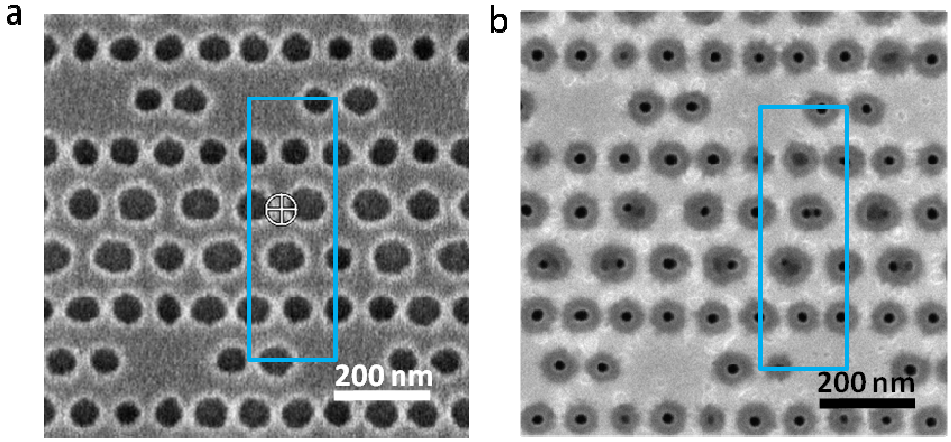

Fig. 5. (a) SEM image of the guiding templates for SRAM, fabricated by 193 nm immersion optical lithography and conventional etching process. (b) DSA patterns in the fabricated guiding templates after removing the PMMA blocks. Single holes are generated inside square templates and hole-pairs are generated in rectangular templates, as designed in Fig. 4. The unit SRAM cell is outlined by blue rectangles. The very few blurred holes in the pattern are possibly a result of electron beam damage during SEM imaging. After Bao *et al*. [6].

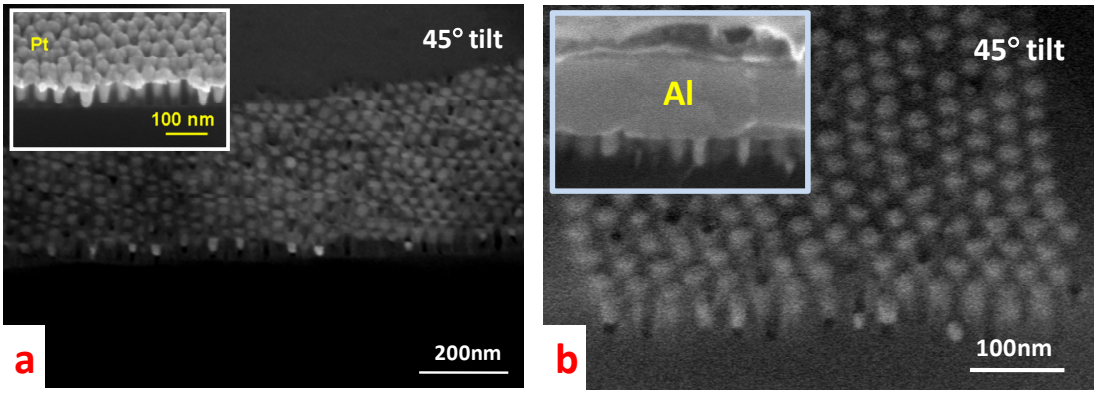

Fig. 6. SEM micrographs showing self-assembled 18nm contact holes in lithographically pre-defined trenches after pattern transfer from PS-PMMA template to inter-layer-dielectric by reactive ion etch. The contact holes are then filled with metals (a) Pt by atomic layer deposition, followed by Al deposition (b) to form electrical contacts. After Chang *et al.* [8].

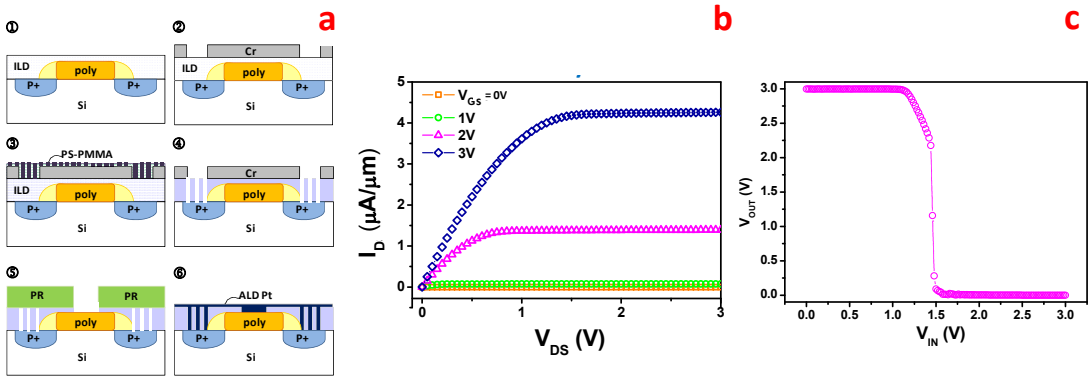

Fig. 7. (a) Process flow for fabricating self-assembled contact holes for contacting the source/drain of a top-gated MOSFET. (b) *I-V* characteristics of the fabricated nFET with nanometer-sized Pt contact holes. The V_T (V_{DS} = -100mV) extracted using the peak gm method is ~0.8V. (c) Transfer curve of fabricated CMOS inverter with 20nm contact holes. V_{DD}=3V. After Chang *et al.* [8].

References

[1] C. J. Hawker, T. P. Russell, "Block copolymer lithography: Merging "bottom-up" with "top-down" processes", *MRS Bulletin* 30, 952-966 (2005).

[2] S. Kim, H. H. Solak, M. P. Stoykovich, N. J. Ferrier, J. J. de Pablo, P. F. Nealey, "Epitaxial self-assembly of block copolymers on lithographically defined nanopatterned substrates," Nature, vol. 424, p. 411 (2005).

[3] C. T. Black et al., "Polymer self-assembly in semiconductor microelectronics", *IBM Journal of Research and Development* 51, 605-633 (2007).

[4] Cheng, J. Y., Rettner, C. T., Sanders, D. P., Kim, H.-C. & Hinsberg, W. D. "Dense Self-Assembly on Sparse Chemical Patterns: Rectifying and Multiplying Lithographic Patterns Using Block Copolymers," *Advanced Materials* **20**, 3155-3158 (2008).
[5] L.-W. Chang, X. Bao, C. Bencher, H.-S. P. Wong, "Experimental demonstration of aperiodic patterns of directed self-assembly by block copolymer lithography for random logic circuit layout", *IEDM*, p. 752 (2010).
[6] X. Bao, H. Yi. C. Bencher, L.-W. Chang, H. Dai, Y. Chen, P.-T. J. Chen, and H.-S. P. Wong., "SRAM, NAND, DRAM Contact Hole Patterning using Block Copolymer Directed Self-assembly Guided by Small Topographical Templates", *IEDM* (2011), paper 7.7, accepted for presentation.
[7] Haran, B. S. et al., "22 nm Technology Compatible Fully Functional 0.1 μm^2 6T-SRAM Cell", *IEDM*, p.625-628 (2008).
[8] L.-W. Chang, T.L. Lee, C. H. Wann, C.Y. Chang, and H.-S. P. Wong, "Top-Gated MOSFETs with Diblock Copolymer Self-Assembled 20 nm Contact Holes," *IEEE International Electron Devices Meeting (IEDM)*, pp. 879 – 882 (2009).
[9] H. Yi, X. Bao, J. Zhang, R. Tiberio, J. Conway, L.-W. Chang, S. Mitra, H.-S. P. Wong, "Contact Hole Patterning for Random Logic Circuits using Block Copolymer Directed Self-Assembly," *SPIE* 2012, submitted.
[10] C. Bencher, H. Yi. J. Zhou, M. Cai, H. Dai, J. Smith, L. Miao, J. Cheng, D. Sanders, M. Tjio, S. Holmes, "Directed Self-Assembly Defectivity Assessment," *SPIE* 2012, submitted.