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EUROCMOSHF: DEMONSTRATION OF A FULLY EUROPEAN SUPPLY CHAIN FOR SPACE IMAGE SENSORS

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I. INTRODUCTION

Europe has currently no full supply chain of CMOS image sensors (CIS) for space use, certainly not in terms of image sensor manufacturing. Although a few commercial foundries in Europe manufacture CMOS image sensors for consumer and automotive applications, they are typically not interested in adapting their process flow to meet high-end performance specifications, mainly because the expected manufacturing volume for space imagers is extremely low. Moreover, the foundry landscape is very volatile and longevity cannot be guaranteed over a long time, as there is a lot of consolidation in the semiconductor industry. This triggered ESA to set up two activities to evaluate the performance of European suppliers of CMOS image sensors. In this paper we report on the first activity, aimed for high-flux space applications, called EuroCMOSHF. The roles of the different partners of the consortium is as follows: CMOSIS designs an image sensor with space specifications, imec is manufacturing the backside illuminated image sensor, and Thales Alenia Space is responsible for the electro-optical characterization.

II. SPECIFICATIONS

In the statement of work of the project, ESA requested a number of specifications typical for a high-flux space imager, such as used e.g. in earth observation applications. The imager had to be monolithic CMOS and backside thinned and illuminated. It should be a global shutter imager, use a pinned photodiode, have a pixel size between 15 and 25 um and an array size which is scalable up to 2048 x 2048 pixels. During the design phase of the project the following target performance specifications were defined:

Imager parameter	**Value**	**Units**
Array size	512 x 512	pixels
Pixel size	20	micron
Fill factor	100	%
Shutter type	global	
Frame rate	40	Hz
Integration time	1 – 5000	ms
Windowing	yes	
QExFF	>50 over 400 – 900 nm	%
MTF	>50 at Nyquist	%
Dark current	< 20	pA/cm^2
Read noise	< 50	e^- rms
Full well capacity	>500	ke^-
Parasitic light sensitivity	< 0.02	%

Table 1: Specifications of the EuroCMOSHF imager.

III. DESIGN

1. Sensor architecture

Starting from the specifications, CMOSIS designed a 512x512 two-dimensional image sensor of which the block diagram is shown in Figure 1. In order to match the requirement of a global shutter in combination with a full well capacity of 500 ke-, a dual-gain voltage-sampling global shutter pixel was used (Figure 2). It allows for true correlated double sampling and good global shutter efficiency in combination with backside illumination and has been implemented before in a demonstrator imager using a commercial 0.18 µm technology [1]. In terms of readout this pixel structure requires a doubled amount of circuitry since each pixel has a high-gain and a low-gain output. The latter results in 1024 readout columns for 512 pixel columns. During Row-Overhead-Time (ROT) the high- and low-gain reset and signal voltages are directly transferred from the pixel columns into the sample-and-hold stages and sequentially buffered onto a reset and signal analog bus. From Figure 1 it is clear that the readout part is split in two identical blocks. Each block has common analog buses and a dedicated analog output stage. The output stage performs correlated double sampling [2] by subtracting the reset voltage from the signal voltage for each gain channel. Further off-chip AD conversion then digitizes the analog output values. The sensor timing is controlled entirely external and, for readout, mainly drives the on-chip decoding and shift register logic. An on-chip register bank (SPI) is foreseen to control various bias settings. A test block allows monitoring a set of on-chip analog and digital signals.

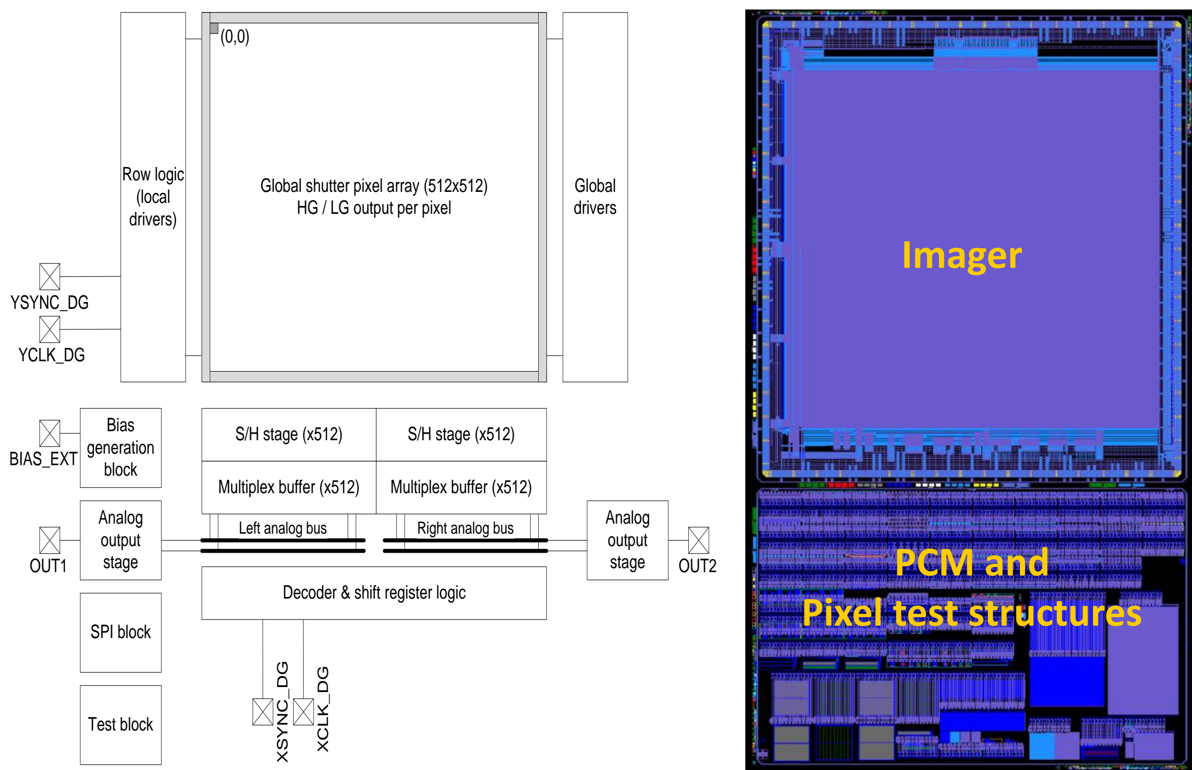

Fig. 1. Block scheme of the EuroCMOSHF imager design (left), layout view (right).

Apart from the imager itself, imec added a number of test structures to the design, in order to evaluate the technology performance: PCM for CMOS (e.g. transistor) devices, and pixel test structures for e.g. dark current and pinning voltage measurement.

2. Pixel structure

The reported dual-gain pixel topology is very similar to [1] and is shown below in Figure 2.

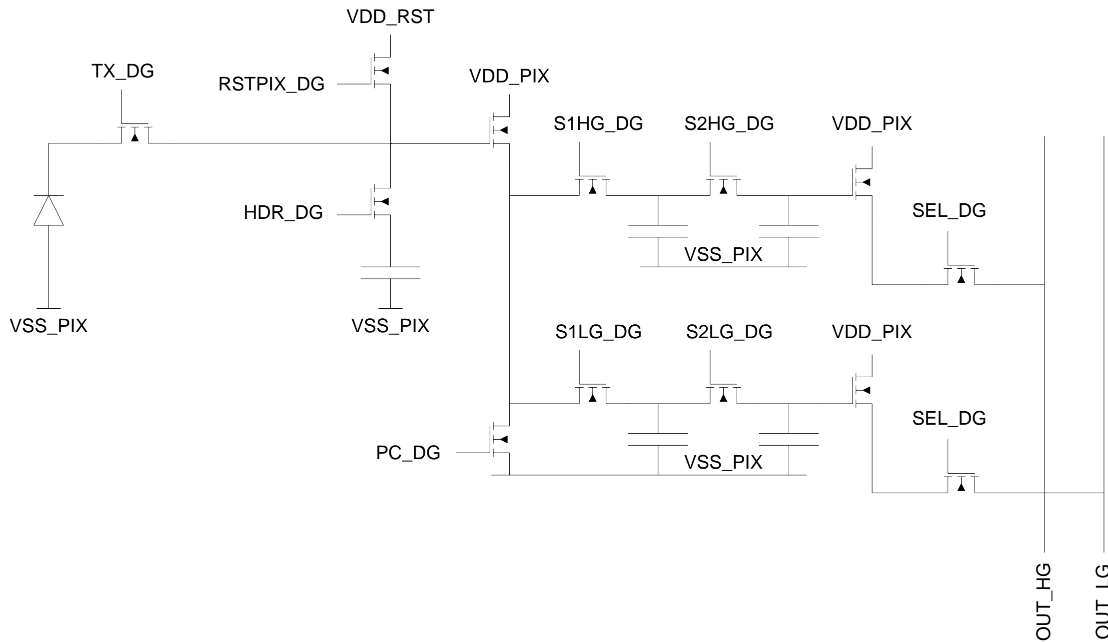

Fig. 2. Topology of the EuroCMOSHF dual-gain global shutter pixel.

The pixel timing during Frame-Overhead-Time (FOT) is shown below. This timing is applied globally to the pixel array, ending the exposure time.

Signal ID	*Applied vectors*
RSTPIX_DG	
S1HG_DG	
S2HG_DG	
S1LG_DG	
S2LG_DG	
TX_DG	
PC_DG	
HDR_DG	
SEL_DG	0

Table 2: Pixel timing during FOT

After disabling the pixel's reset state the low-gain reset value is stored with the S2LG_DG control signal. Disabling the HDR switch decreases the floating diffusion capacitance, moving the pixel into high-gain mode. The corresponding reset level due to this action is stored using S2HG_DG. During a first transfer pulse the collected charge on the pinned photodiode then lowers the voltage on the floating diffusion capacitance. After settling, this high-gain signal voltage is stored with S1HG_DG. At sufficiently low light levels *all* photo charges will have been transferred to the floating diffusion capacitance, while for large charge packets this transfer may be incomplete. Indeed, charge transfer halts when the voltage on the floating diffusion capacitance drops below the pinned photodiode's pinning voltage (thereby saturating the high-gain channel). Therefore, for a second, low-gain reading, the capacitance on the floating diffusion is increased again, now allowing a full low-gain charge transfer during a second transfer pulse. The latter is possible because the voltage on the HDR capacitance is close to the reset voltage, prior to connecting it to the low capacitance of the floating diffusion (charge sharing). The corresponding low-gain signal level is stored using S1LG_DG. The combination of floating diffusion capacitance and switched HDR capacitance is designed carefully as to prevent saturation during that second transfer. Once all reset and signal levels have been stored in the in-pixel capacitances, the FOT ends by resetting the floating diffusion voltage. It remains reset during the subsequent exposure time.

IV. TECHNOLOGY

Although not a commercial foundry, imec has a 130 nm CMOS process on 200 mm Si wafers, which was enhanced with a CMOS image sensor (CIS) module and an embedded CCD-in-CMOS (eCCD) module [3]. Also dedicated imager post-processing of e.g. Fresnel type micro-lenses [4] and hyperspectral filters (both at pixel level) [5] are available. Contrary to commercial foundries, imec is flexible in adapting the process flow in order to meet high-end imager customer requirements. Examples are the use of engineered epitaxial substrates (e.g. to enhance charge collection and reduce cross-talk) and stitching (in order to realise large area imagers). The imec offering includes imager design, technology development, prototyping and low volume manufacturing, as well as space qualification services.
Imec's CIS technology features a dual gate module (1.2V and 3.3V) and MiM capacitors with a capacitance of 1.1 fF/um^2 (Fig. 3). Inside the pixel, a pinned photodiode process module as well as an optimized transfer gate are available, as well as low V_t transistors. Imagers with 3T and 4T type of pixels have been designed with a pixel pitch of 2.5 micron and higher, a conversion factor of up to 70 microVolt/e$^-$ and a noise of a few electrons. Both global and rolling shutter imagers, eventually with transistor sharing, as well as radiation hard pixels have been designed. A large effort has been dedicated to the reduction of dark current, e.g. by reducing and or gettering of metal contaminants. Currently on large test photodiodes values as low as 20 pA/cm^2 are obtained for frontside illuminated imagers. Dark current reduction for backside illuminated imagers is ongoing. For a maximum sensitivity, a backside illumination process module has been developed. Several antireflection coatings optimized for visible as well as near-UV sensitivity are available [6].

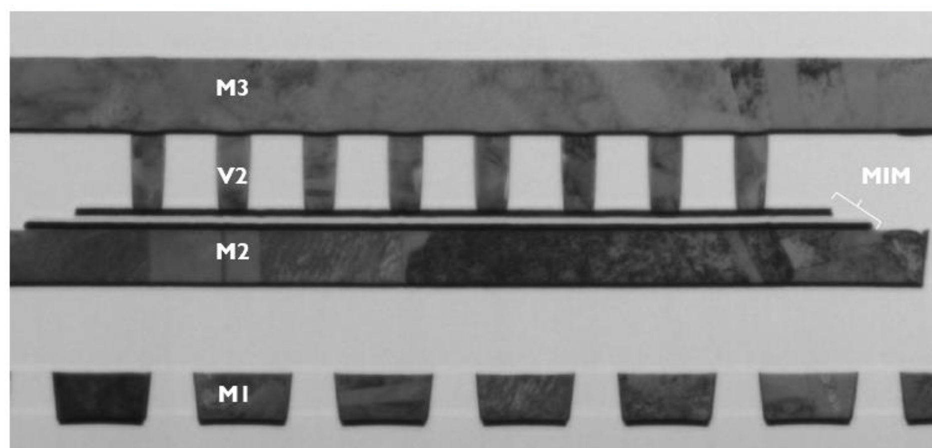

Fig. 3. Cross-section of the back-end-of-line stack of the imec 130 nm CIS process, including a MiM capacitor.

The imec technology used for the EuroCMOSHF device is the 130 nm CMOS image sensor process processed on 200 mm wafers in Leuven, Belgium. In order to meet the quantum efficiency imec's backside illumination process will be applied. In combination with an anti-reflection coating optimized for the visible, this will result in a QE higher than 70% over the full visible wavelength range. The use of a graded thick epi (final thickness after thinning ~ 15 um) ensures a high (near infra-)red response in combination with a low pixel-to-pixel cross-talk. In order to minimize the dark current, the latest dedicated process developments at imec were implemented using process splits.

V. RESULTS

In order to check the performance of both CMOS and pixels, dedicated test structures have been measured, both after finishing the first metal and after the completion of the frontside illumination (FSI) processing. The PCM structures measured included transistor parameters such as I_{on} and I_{off} current as well as Kelvin and chain devices to check (contact) resistance data. All parameters were found to be within the standard 130 nm CMOS specifications. The MiM yielded a capacitance of 1.1 fF with an acceptable leakage current. More specifically for the pixel, transistors with low threshold voltage were measured and found to be in spec. The pinning voltage of the pinned photodiode was measured to be close to the target value (1.5 V). Currently the wafers have passed successfully the frontside processing. At the time of writing the frontside processed imagers are in debug phase at CMOSIS.

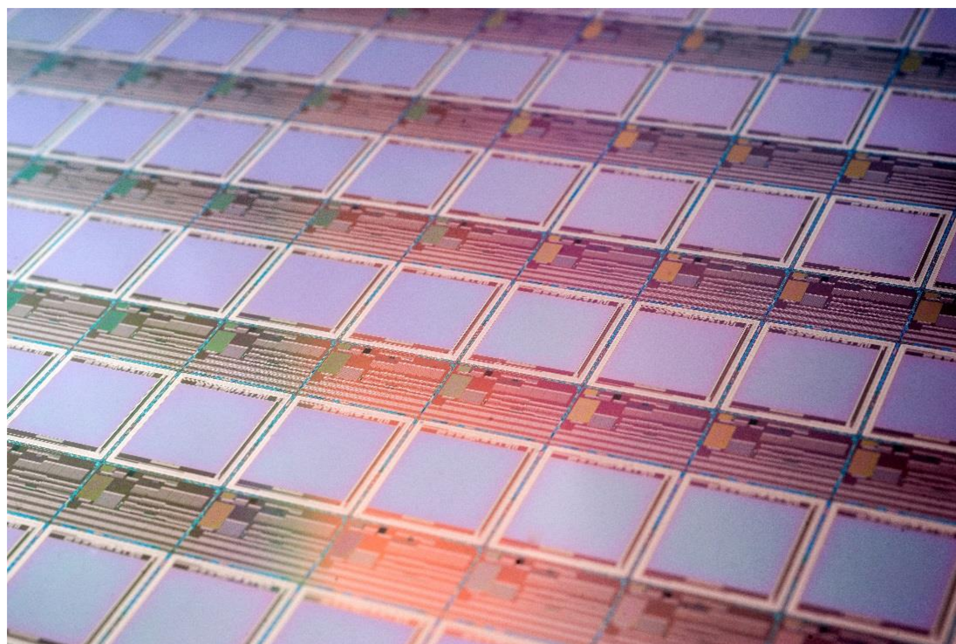

Fig. 4. Picture of a 200 mm wafer with the EuroCMOSHF devices and test structures.

VI. OUTLOOK

After full characterization of the frontside illuminated imagers, imec will continue to process the backside illumination process module, including wafer-to-wafer bonding, thinning and backside passivation, anti-reflection coating and bond pad opening. Backside radiometric characterizations will be performed by Thales Alenia Space on a dedicated high-precision test bench. Light is generated by a halogen lamp with well-defined spectral characteristics. A set of filters and diaphragm can tune the spectrum and light intensity to be injected through an integrating sphere. The spatially uniform output optical signal feeds a light sensor to monitor the optical source radiance. The detector is enclosed in a black box to avoid stray-light. The control of the equipment and boards, such as the control of the optical source and power meter, is carried out by a customized LABVIEW software, using different communication ports (USB, GPIB, RS232). The measurements themselves include the characterisation of the Fixed Pattern Noise (FPN), the dark current and noise, the Dark Signal Non-Uniformity (DSNU), the Pixel Response Non-Uniformity (PRNU) over the whole array and for 6×6 pixels clusters, the non-linearity behaviour, the Full Well Capacity (FWC), the quantum efficiency including the Fill Factor (QE×FF), and the Modulation Transfer Function (MTF) inside the 350-800 nm spectral range. The MTF measurement will be static and based on the knife edge method. In a next phase the full space qualification (including radiation testing) of imagers realized in this European supply chain needs to be addressed.

REFERENCES

[1] G. Meynants, G. Beeckman, K. Van Wichelen, T. De Ridder, M. Koch, G. Schippers, M. Bonnifait, W. Diels, J. Bogaerts, ‘Backside illuminated 84 dB global shutter image sensor’, Proc. 2013 Scientific Detector Workshop, Firenze, 7-11 October 2013

[2] G. R. Hopkinson and D. H. Lumb, “Noise reduction techniques for CCD Image Sensors”, J. Phys. E, Sci. Instrum., Vol. 15, No. 11, pp. 1214 – 1222, Nov 1982

[3] Pierre Boulenc, Jo Robbelein, Linkun Wu, Luc Haspeslagh, Piet De Moor, Jonathan Borremans and Maarten Rosmeulen, ‘High speed TDI embedded CCD in CMOS sensor’, Proceedings of this conference: ICSO 2016

[4] V. Rochus, X. Rottenberg, I. De Wolf, P. Soussan, and P. De Moor, ‘Pixel performance enhancement by integrated diffractive optics’, Proceedings of IISW 2015

[5] Andy Lambrechts, Pilar Gonzalez, Bert Geelen, Philippe Soussan, Klaas Tack and Murali Jayapala, ’A CMOS-compatible, integrated approach to hyper- and multispectral imaging’, Proceedings of IEDM 2014

[6] K. Minoglou, D. San Segundo Bello, D. Sabuncuoglu Tezcan, L. Haspeslagh, J. Van Olmen, B. Merry, C. Cavaco, F. Mazzamuto, I. Toqué-Trésonne, R. Moirin, M. Brouwer, M. Toccafondi, G. Preti, M. Rosmeulen and P. De Moor, ’A platform for European CMOS image sensors for Space’, Proceedings of ICSO 2014