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Linear CCD array TH-7834B performances near 10 MHz

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The spatial resolution improvement of Earth observation satellites implies higher CCD readout frequencies (at the moment for an instrument such as SPOT 5, typical CCD readout frequency reaches 5MHz for an Earth resolution of 3.5 m and a 60 km swath). Soon, as we try to increase the spatial resolution without degradation of the swath, reading frequency of 10 MHz will be required. Furthermore, this output data rate needs to be achieved with Correlated Double Sampling (C.D.S) which remains the only way to deliver good performances in term of signal-to-noise ratio.

This poster shows results of measurements at 9.25 MHz readout frequency on a linear CCD array ATMEL TH-7834B, already used in spatial instrument SPOT 5 at lower frequencies.

The most important parameters to measure were :

- the shape of the CCD output signal, to determine the length of the area available to sample the signal,
- linearity and transfer efficiency, with respect to the irradiance of the CCD,
- the stability of the performances in case of phase shift of the CCD and acquisition clocks.

Measurement bench

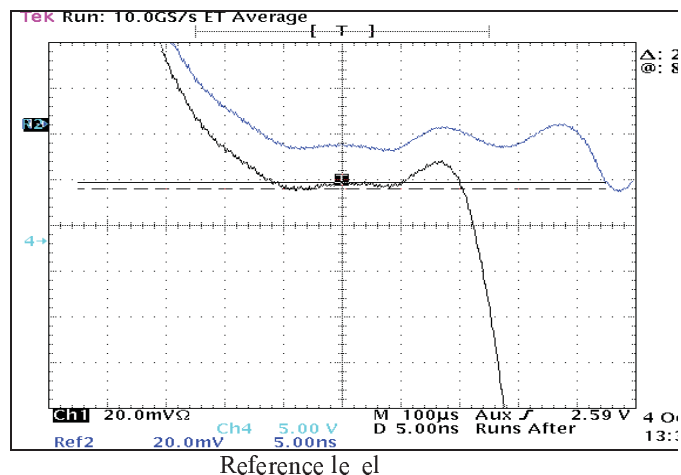
First of all, precise measurements require a bench to catch CCD signal et measure the linearity error.

A specific electronic was designed, to allow a maximum bandwidth, and a fine tuning of the CCD clocks was performed, to optimize the shape of the output signal. Our video chain was measured for a differential non linearity of +/- 0.3 LSB, and a global non linearity of 2 LSB (with a 12 bit resolution) at 10 MHz frequency.

CCD signal shape

The following figures show the reference and video levels at 9.25 MHz, both for a dark pixel, and an illuminated pixel. They exhibit a useful length of more than 10ns for the sampling.

Some improvements of the CCD internal output amplifier are possible to more improve the speed and reduce the ripple of the output signal.



The problem is obviously : How precise have to be the clock phases, in order to maintain a long enough length for the video and reference level ? In other words : what kind of drift is authorized for the slope of the clocks (of the CCD and of the acquisition chain) ? The following paragraphs give some answers to this question.

Linearity

We tested the degradation of the linearity between pixels at 5 MHz and pixels at 9.25 MHz

Linearity error is given by

$$NL(\%) = \left(\frac{V_{ccd} - V_{obsc}}{V_{ccdf} - V_{obsc}} \frac{E_{clref}}{E_{cl}} - 1 \right) \cdot 100$$

where

- V_{ccd} (resp V_{obsc}) is the result of a CDS (Correlated double sampling) of the CCD signal for illuminated pixels (resp dark pixels),
- E_{cl} is the irradiance on the illuminated pixels (in W/m²),
- the "ref" values are referenced to the middle of the dynamic (here 500 mV for V_{ccd}).

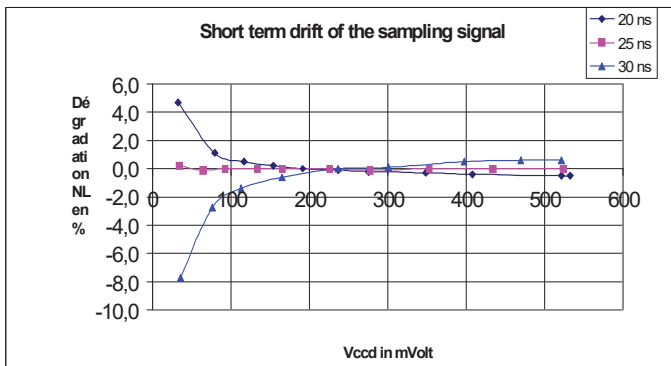
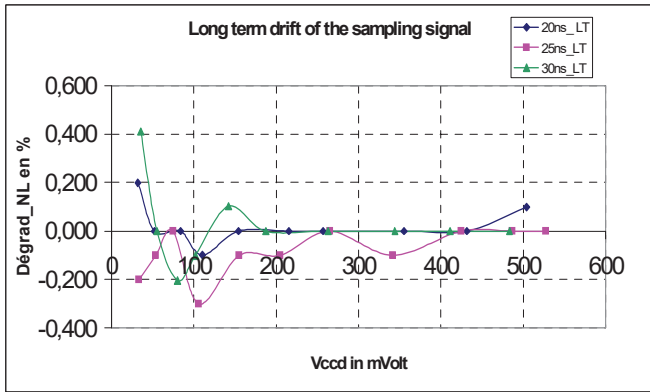
The issue was of course to know what kind of margin existed for the clock signals, in order to maintain the linearity error at low level.

So we simulated 2 kinds of time shift of the sampling clock signal :

- a long term shift, simulated with a similar shift applied to illuminated pixel and dark pixels : this case simulate a long term shift in orbit, due to thermal phenomenon, or radiation effects,
- a short term shift, simulated with a shift applied only to illuminated pixels, when dark pixels was sampled with the optimized clock phase : this case simulate the short term jitter, which is generally very small and well characterized by ground measurements.

The results are the following for the sampling signal of the CCD video level. The curves are given :

- with respect to the total CCD level ($V_{ccd} - V_{bc}$),
- for 3 different delay of the sampling signal: the middle one is the best



The larger sampling time of 10 ns affects the linearity, even at low signal level: so the authorized shift for the sampling signal can be

A shorter sampling time induces a fast degradation of the linearity at low level. Hopefully, in the currently used acquisition chains, this short term jitter is very low, and its drift increase dramatically in orbit

Similar investigations have been carried out for the other clock (sampling signal for frame level, CCD clock), leading to similar results:

- longer term drift affects 10 ns architectures with a significant degradation of the linearity,
- shorter term jitter has a tight budget and is

Transfer inefficiency

The degradation of this parameter has been observed for clock frequencies between 5 MHz and 9.25 MHz