Lithography strategies for 180 nm CMOS device fabrication

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Abstract

Progress in optical lithography continues to pace the development of high speed microprocessors and high density DRAM and flash memories. Continuing progress by optical lithographers has allowed low-cost, volume manufacturing of sub-0.25 micron, high density CMOS devices. With stunning success, entire computer systems are now being placed on a single chip, enabling new, advanced technologies for computation, communications, and entertainment to flourish. This paper will outline the requirements of lithography envisioned in the National Technology Roadmap for Semiconductors currently being renewed for 1997 publication. A possible path for the evolution of optical lithography to 180 nm, and then to 130 nm, is mapped out, allowing promising technologies such as 1X proximity x-ray, extreme ultraviolet projection (EUV), scanning projection electron beam (SCALPEL), or ion projection (IPL) to mature in time to address 100 nm and below.

Pull in of the Lithography Roadmap

For more than 30 years the timing for introducing new generations of device density has followed Moore's Law : the number of transistors per chip doubles every 18 months. The NTRS or "SIA Roadmap" is based on Moore's Law (1). In order to meet the increased worldwide demand for higher performance computation and communications products, the steady reduction of lithographic feature size in IC production has accelerated in recent years and has become a headlong rush. In the three years since the last Roadmap was published (2), the introduction of 0.25 micron has been pulled in one year, from 1998 to 1997, and the introduction of 180 nm is now forecast for 1999, two years earlier.

A good example of the accelerated roadmap is the rapid reduction in gate length of CMOS logic devices, needed to drive the increased performance of microprocessors. Processor speeds have tripled over the last three years in fierce market competition. In many cases the lateral scaling of dimensions has not been accompanied by a similar scaling in the vertical due to the requirements for interconnect performance and reliability. Thus structures of extraordinary density and relatively high aspect ratio must be patterned, inspected, and measured. This trend has put strain on IC lithographers, lithographic equipment and material suppliers, metrologists, and mask suppliers.

To sustain this pace, the cost of optical lithography has escalated rapidly and, with the increase, a crisis has continued to loom. Unless there is international cooperation among integrated circuit makers, equipment suppliers, and material suppliers, to devise a

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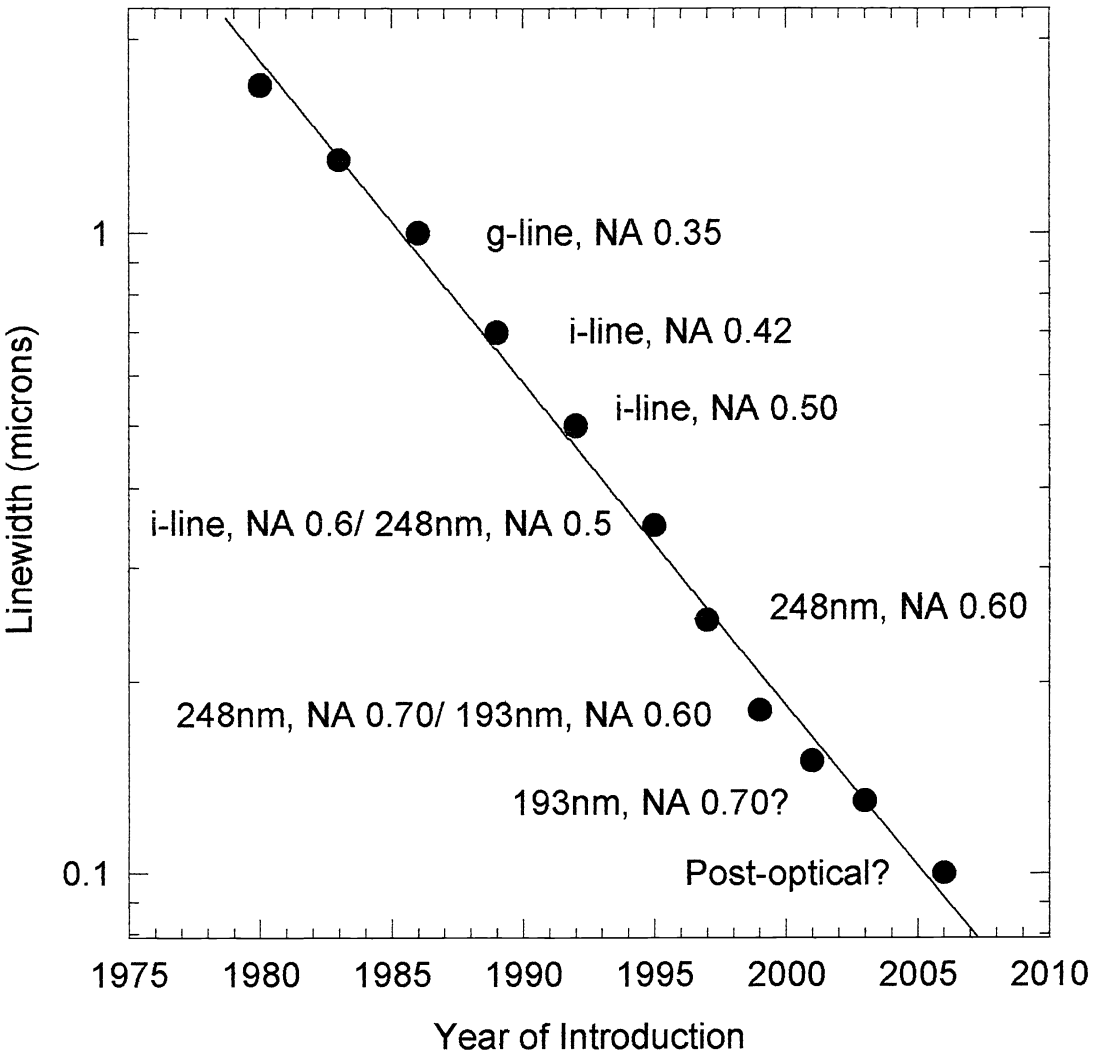

Figure 1 - Reduction in minimum linewidth with time, 1997 NTRS.

workable strategy for developing new lithography technologies, within the total investment envelope, IC manufacturing will fall behind the Roadmap's schedule and industry growth will slow.

KrF Lithography for 250/180 nm Design Rules

In 1997, leading edge IC manufacturers are putting 250 nm design rule 64M DRAMs and sixth-generation microprocessors into volume production using 248 nm DUV lithography. 250 nm design rules generally mean 600-700 nm pitch in logic and 500-600nm in memory. Gate widths are shrinking to 200 nm and below, to support 300+MHz processors.NA 0.60, 248 nm (KrF excimer laser) steppers and scanners are being introduced to handle these jobs. Naturally, IC makers will attempt to push these tools to address the first round of development for 180 nm technologies.

By the end of 1999, device geometries will again shrink and 180 nm lithography will be required. Since 193 nm (ArF excimer laser) step-and-scan tools and resist processes will not be mature in time for the initial insertion of 180 nm production, lithographers will have to stretch 248 nm processes, the first time sub-wavelength imaging will be used in volume production.

Sub-wavelength imaging puts particularly strict requirements on the mask maker. As one approaches the resolution limit of an optical system, the linearity between mask and wafer CD s breaks down. Small deviations from the design linewidth on the reticle can lead to magnified variations on the wafer. Thus the requirements for CD uniformity across the reticle as well as the allowed mean-to-target error must both be tightened further from the values derived from simple scaling of 250 nm specifications. From the stepper supplier's end, 0.7 NA lenses are needed to help compensate for less-than-adequate CD control on reticles.

The use of optical proximity correction and phase shifting techniques will also expand as low k-factor imaging becomes more common. This will have significant impact on the complexity of the maskmaker's job, as well as on the economics of the business. Larger data volumes and longer write times can be expected. Defect inspection and repair for subresolution assist features and phase shifting elements will present formidable challenges. The integration engineer, layout engineer, microlithographer, and maskmaker will have to work closely together to produce reticles which will support 180 nm lithography.

Wavefront engineering and gate reduction etch techniques can be used to push 248 nm lithography to 180 nm. Logic gates will probably be the first features printed at 180 nm. 248 nm lithography using a phase edge approach can be used. Strong phase shifting is now being used for microprocessor production at i-line and can be adapted to 248nm. Initial application of 193 nm will be in comparison to what can be achieved at 248 nm with tricks. Memory technology requires more time to mature. Sophisticated approaches using

off-axis illumination and/or PSM may allow 248 nm to address most, if not all, layers of the first generation of 180 nm memory production.

ArF Lithography for 150/130nm Design Rules

ArF (193 nm) lithography is being developed but production-worthy tools will not appear until 1999 or 2000. As we have seen, this means the first phase of 180 nm production will have to be done at 248 nm. Extension of 248nm lithography to 150 nm may also be required depending on the status of developments in 193nm.

Development of 130 nm technologies has started at several locations, using research lithography techniques (direct ebeam write, for example), but will not be able to progress rapidly until the first 193nm full-field tools appear. As 193 nm prototyping capability at 200mm becomes available from the stepper suppliers in late 1998/early 1999, IC makers will attempt to use it for 150 and 130 nm gate level production on logic. As there is no alternative that will be ready in time, the 130 nm generation will be ArF's.

Once the shift to 193nm has occurred, there will be enormous pressure from IC makers to extend its use another generation. The question now for optical lithographers should be: can 193nm lithography be pushed to 100nm? 100 nm logic gates on 130 nm design rules can be expected for production by 2003. 193nm lithography will be expected to support this level of miniaturization.

Memory production at 150 nm will probably wait until 300 mm equipment is available before big investments in 193 nm are made. ArF shrinks of the 1Gbit DRAM may be first seen in production by 2000 or 2001 if development progresses without major problems. Further memory shrinks to 130 nm can be expected by 2002/03.

Lithography Requirements for Logic and Memory Manufacturing

The lithography requirements for logic and memory manufacturing are quite different. Memory (DRAM, SRAM, flash EPROM) manufacturing requires the ultimate in packing density in order to get the smallest die size (which leads to the lowest manufacturing cost). Lithography for memory is extremely challenging for resolution and pattern overlay. Core arrays lend themselves to frequency-doubling techniques (alternating PSM, off-axis illumination). DRAM production remains the driver of stepper technology. While the microprocessor business can be very profitable compared with memory, the worldwide microprocessor business is less than 20% of the worldwide memory business in volume. DRAM die sizes will continue to grow, though the trend forecast in the newest Roadmap is slowing as emphasis is on shrinking minimum feature and the minimum cell size at a more rapid rate.

Logic devices are not as tightly packed as memory, but gate width is squeezed in order to increase operating frequency. Linewidth control of the gate is the key issue. Die size is largely controlled by interconnect pitch, in which overlay is an important factor.

Microprocessor die sizes are currently in the 100-200mm2 range, and the rate of increase has slowed. Gordon Moore has recently estimated the cost of building microprocessors as in the neighborhood of $1billion per acre of silicon and has stated that this puts effective limits on the maximum die size (3). Here, manufacturers build more functionality (add more transistors) by shrinking minimum feature size and adding interconnect layers in addition to increasing die size. Damascene processing with copper interconnect may replace direct metal patterning, in order that processor speed not be limited by interconnect delays.

Why is it so important to improve CD control for logic devices? The chief reason is the key importance of controlling gate length in high speed CMOS transistors (4). Microprocessor speed is one of the most important determinants of the price that an IC maker can get for the part. The microprocessor's speed results from a combination of circuit design and process technology. Of key importance to the process technology are the gate delay, the time it takes a single transistor gate to switch on or off, and the transistor drive current. Both gate delay and drive current are proportional to the inverse of the gate length.The shorter the gate length, the less time it takes an electron to run from source to drain, allowing the transistor to switch. The effective gate length is largely determined by lithography and etch (micropatterning) process capability and control. It is not enough to have a short gate length. All gate lengths have to be tightly controlled across the full chip in order that the timing of signals can be well-correlated and placed in sequence.

A particularly effective way of patterning small gate dimensions is through the use of the Levenson phase edge. The phase edge can produce a sharp aerial image of a semi-isolated or isolated line, of limiting width 0.25 lambda/NA (5). In order to use the phase edge in positive resist, a scheme for eliminating printable phase transitions must be developed. One method is to use a trim mask approach, in which phase transitions that print are removed by the exposure of a second mask, designed for that purpose. Another method, developed by John Nistler at AMD (6), is to use a three phase transition, 60/120/180 degrees, in which 60 degree transitions don't print. This works particularly well for the semi-isolated logic gate layout. The CAD layout for the phase edges can be keyed to transistor layout over active regions, as developed by Chris Spence at AMD (7). With 248nm lithography, gate widths down to 100 nm and below can be printed using a phase edge approach.

The challenges for gate CD control are numerous, and are not limited to control over lateral dimensions, but also to length. Gate overlap of the active region requires that line ends do not shrink back appreciably due to defocus or etch, otherwise unacceptable leakage currents will develop. As the k-factor shrinks to 0.5 and below, diffraction effects tend to shorten gates along their lengths. Optical proximity correction (OPC) algorithms are under intensive development across the industry to control line end pullback and corner rounding.

Another challenge for logic lithography are the new requirements for definition of damascene interconnect layers. Long trenches and holes are required to be printed simultaneously, allowing etch to create high aspect ratio openings in a thick dielectric, which are then filled with the metal film (W, Al, or Cu) and polished. OPC is required to make the exposure windows for long trenches and small vias overlap. 0.2 micron contact holes in 1 micron of dielectric can be expected for production before the end of the century.

0.15 micron gates can be expected in microprocessor production before the end of the century, with 0.13 micron gates in 2001. For gate linewidth, SEM CD metrology needs to provide good correlation with device performance as well as heroic levels of dimensional stability of the order of a few nm.

Overlay budgets will fall to less than 50 nm for device production at the beginning of the new century, placing demands on registration metrology to supply results with better than 10 nm repeatability.

Requirements of Reticle Technology

Reticle technology will become a major focus of interest in the coming years as its contribution to the overall error budgets for linewidth control and overlay become dominant. As we push optics to lower k-factors, printdown from reticle to wafer is non-linear so that small errors in CD on the reticle are "magnified"(8). A 50nm range on the reticle may transfer to the wafer as a 25nm range, instead of 12.5 nm as would be expected from 4X reduction. An accelerated need for improvement in reticle CD control and linearity can be anticipated. This and other technical issues will stress the relationship between reticle supplier and IC maker.

In the US, most IC makers buy reticles commercially. In order to ensure supplies of critical level reticles, new business models have developed.The Reticle Technology Center (RTC) has been created by AMD, Micron, Motorola, and Dupont Photomask to establish a semi-captive supply for advanced technology reticles, at less cost than each member building and maintaining a captive shop. At the same time, DPI can invest in more capital equipment than it would be able to afford on its own. It can also can tap the expertise of the chipmakers' engineers in process development, e.g., for dry etch for oxide or chrome.

Phase shifting technology seems to have stabilized into two principal forms: alternating (aka strong, or Levenson) for isolated gates or dense arrays, and attenuated (aka halftone) for small openings.

For Levenson-type masks, the three-phase approach has been demonstrated to work by AMD printing 300 nm gates with i-line steppers in volume microprocessor production (7). At 248 nm this approach may allow the definition of 150 nm gates, and 100 nm gates with 193 nm exposure in future device production. Inspection and repair for 60 degree phase defects still requires more development. Currently, a defect-free reticle is required.

Various technical issues with attenuated PSM have been resolved, and these are now in wide use throughout the industry. Attenuated blanks for i-line and 248nm are commercially available, and blanks for 193nm lithography are being developed.

Optical Extensions beyond 193nm

Since the history of optical lithography has seen Moore's Law supported by the succession of one shorter wavelength after another, it is natural to ask: why not develop another wavelength even shorter than 193nm to address 100nm device production? Indeed, some workers have advocated research into lithography at 157 nm, where the F2 excimer laser could provide a strong lithographic source, or at 126 nm, using an Ar dimer source.

Fused silica does not transmit light below ~190 nm efficiently, so a refractive or catadioptric lens for 157 nm would have refractive elements made entirely from CaF2, while reticles could be built from CaF2 or sapphire. It is not clear at this time whether CaF2 quality and polishing techniques will improve enough over the next two or three years to make this a possibility. As for fully-reflective systems, diffraction-limited designs with lithographically useful field sizes do not achieve high enough NA s to be substantially superior to high NA 193 nm capability.

At 126nm, no glass material transmits light, so the lens must be fully reflective, using aluminum mirrors coated with aluminum oxide. Again the high NA design restriction makes it questionable whether this represents a substantial improvement in resolution or depth of focus compared to 193nm. In addition, the source at 126 nm is reported to be very difficult to build, operate, and maintain. Below 120 nm, aluminum no longer reflects ultraviolet, making the fabrication even of reflective lenses impractical.

Considering the relatively small improvements offered in resolution for these new wavelengths, it is questionable whether it makes economic sense to develop them. Since the industry demands at least two generations from any new lithography technology, one must also consider carefully whether 157 nm or 126 nm lithography could be stretched to produce devices at 70 nm design rules (with gates as small as 50 nm wide). A recent workshop organized by Sematech concluded that it would cost nearly as much money to develop 157 nm lithography as it would to develop EUV lithography, with much less prospects for ultimate extension to 50 nm device fabrication.

Post-optical Alternatives

There are several technologies which have been developed in sufficient depth to claim the potential as a successor to optical lithography.

Extreme Ultraviolet Lithography (EUVL) - 4X reduction projection scanning at 13nm photon wavelength. Uses MoSi resonant reflector mask blanks, refractory metal absorber. TSI resist process required.

1X proximity X-ray lithography (PXRL) - 1X proximity printing at 1nm wavelength. Mask : Refractory metal (TaX) absorber on SiC membrane. Exposure of 0.5 um thick DUV resists (APEX, UV4) have produced 100 nm L/S, with doses in the range 80-200 mJ/cm2.

Projection electron beam lithography (SCALPEL) - 4X reduction projection scanner operating at 100kV. Strutted mask structure with refractory metal (W/Cr) scatterer on a Si3N4 membrane. 0.4 um thick DUV ARCH resist has been exposed at ~15 uC/cm2 to produce 80 nm L/S.

Ion projection lithography (IPL) - 4X reduction projection stepper operating at 75 kV, using hydrogen or helium ions. 80 nm L/S have been resolved in 0.37 um Shipley UVIIHS DUV resist. Silicon stencil mask, 2.5 um thick membrane. Pattern specific emulation may be required, as in 1X x-ray mask fabrication. Two stencil masks per layer are needed for active, gate, and interconnect layers, in general.

Conclusions and challenges

To keep up with the daunting pace of Moore's Law, micropatterning engineers are forced to adopt new lithographic technologies before they have had time to develop fully. Lithographers need many simultaneous improvements in stepper resolution and overlay, resist performance, metrology, and in mask technology.

248 nm optical lithography is being introduced across the world to produce 250 nm generation memories and microprocessors. Use of off-axis illumination, OPC, and phase shifting reticles will allow the extension of 248 nm to about the 150 nm level.193 nm optical lithography is in development and is expected to be introduced for device production at the 150 nm level (2000 logic, 2001 memory) and to extend to 130 nm, and further to 100 nm.

The industry faces a discontinuity at the 100 nm level as the contrast of 193 nm images goes to zero. Further development of optics, to 157nm or 126 nm, does not offer extension to 50 nm resolution and below as is needed for the successor to 193nm and is probably not cost-effective.

The development of a post-optical path must gain industry attention and consensus. The next technology must be capable of extension to 50 nm. A cooperative decision making process is being sponsored by Sematech, with international participation considered essential.

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