Metrology challenges for double exposure and double patterning

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ABSTRACT

Double patterning has emerged as a likely lithography technology to bridge the gap between water-based ArF immersion lithography and EUV. Water immersion, single exposure lithography is limited to about 40nm half pitch with NA 1.35. Extension of immersion with high index fluids and glasses is theoretically possible, but faces severe challenges in technology, economics, and timing. In order to extend water immersion lithography further, much attention is given to reducing effective k_1 to less than 0.25 using double patterning. This paper explores the unique challenges IC metrology faces to enable double patterning, first in development, then in production.

1. Introduction

The introduction of double patterning is driven by the accelerated timing of the introduction of device shrinks below 40nm half pitch, especially for NAND flash. This has resulted from differences in the layout of various devices, as will be shown in Section 2. Likely lithographic technologies for 32nm half pitch will be reviewed in Section 3. The resolution limits of single exposure, double exposure, and double patterning lithography will be reviewed in Section 4. Error budgets for SE, DE, and DPT will be reviewed in Section 5. The special metrology requirements for double patterning will be discussed in Section 6. Active compensation schemes to provide more process window for double patterning will be covered in Section 7.

2. Divergence of Roadmaps: Memory and Logic

The limits of optical resolution in lithography are dictated by the Rayleigh equation $R = k_1 \lambda / NA$, where k_1 is a proportionality factor which has a limiting value of 0.25 for a single exposure, λ is the wavelength of the light and NA is the numerical aperture of the optics (1). As k_1 decreases, contrast is lost in the image. Resolution enhancement technology (RET) has evolved to bring back contrast even as device half pitch has continued to shrink. Common RETs employed include off-axis illumination and the use of phase shifting masks and the addition of sub-resolution assist features to mask features (2).

Memory devices have core areas which are highly periodic arrays of common geometries, repeated on certain fixed pitches. Such arrays lend themselves more easily to RETs such as strong cross pole or dipole illumination. As a result the limit of resolution defined by Rayleigh's equation can be more closely approached. Further, NAND flash devices have simple one-dimensional structures such as wordline arrays separated by a simple string of contacts, while DRAM must have one contact and one capacitor printed per cell, requiring complex 2D imaging. As a result, NAND devices can be printed with $k_1 \sim 0.27$-0.29, while DRAM is limited to ~ 0.29 to 0.31.

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Advanced logic devices have a mixture of periodic memory structures, typically 6T SRAM cache, and areas of random logic. While efforts are made in DFM to make features "litho-friendly", retaining the mixture of complex 2D geometries presents a difficult problem for optimized imaging and limits the possible k_1 to around 0.4 and above.

As a result of these differences in imaging, NAND flash can be printed on a finer half pitch than can advanced logic devices, using the same scanner technology. The characteristics and implications for lithography of different devices are shown in Figure 1.

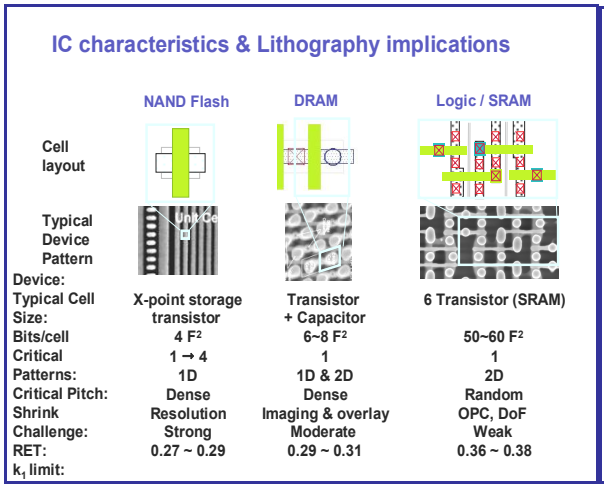

Figure 1: IC characteristics & Lithography implications

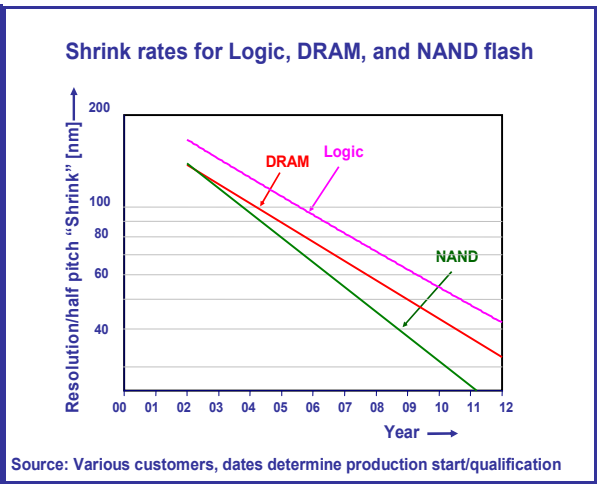

Figure 2: Shrink rates for Logic, DRAM, and NAND flash

Memory manufacturers have the greatest pressure to reduce feature size in order to decrease cost per bit. While the memory content of many advanced logic parts such as DSPs and microprocessors hovers around 50% of die area, these devices can not be printed at the same minimum half pitch as pure memory due to the imaging restrictions dictated by the mixture of feature types. Thus memory devices and, in particular, NAND flash devices have become the principal driver of the lithographic shrink. The average shrink rates of NAND flash, DRAM, and advanced logic devices are illustrated in Figure 2. This data was collected from 14 major IC makers and plots the minimum half pitch versus the date of introduction to volume manufacturing.

3. Likely Lithographic Technologies for 32nm

From the Rayleigh equation, there are three levers to improve optical resolution: 1) increase NA, 2) decrease wavelength, or 3) decrease k_1. Figure 3 indicates the path which optical lithography has taken to address the 65 and 45nm half pitch nodes, illustrates the issues at 32nm, and forecasts the likely path beyond 32nm (assuming device scaling itself continues, a subject beyond the scope of this work). Across the top are the half pitch nodes and the dates of their earliest introduction to production assuming a two-year cycle. Along the vertical axis are the wavelengths and numerical apertures which have been introduced or are contemplated to address these half pitch nodes. Along the diagonal are the corresponding k_1 values.

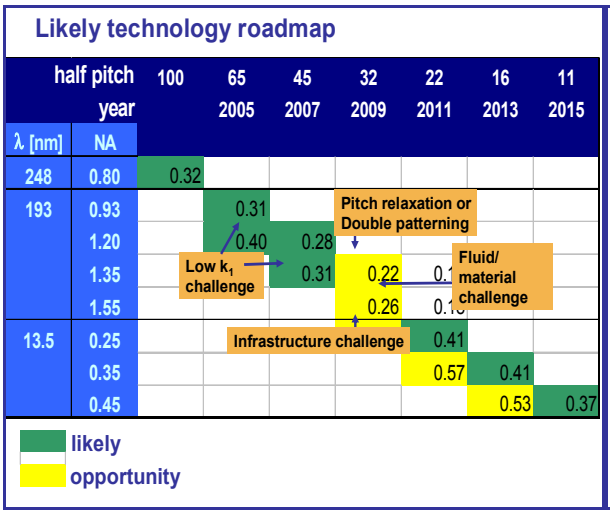

Figure 3: Likely lithographic technology roadmap.

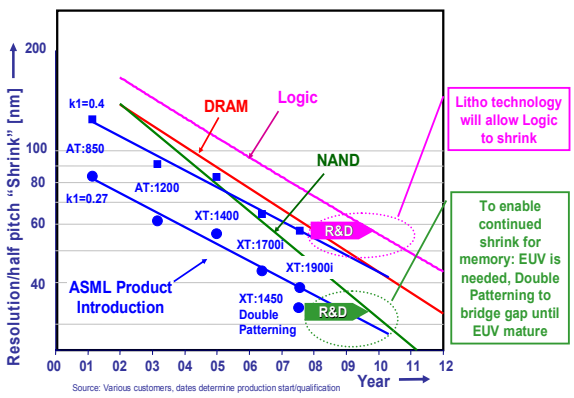

Figure 4: Shrink rates for Logic, DRAM, and NAND flash versus tool introduction at k_1 0.27 and 0.40

At 45nm half pitch, volume production lithography is enabled by hyper NA water immersion scanners operating at 1.35NA and 193nm wavelength. At 32nm, single exposure water immersion is no longer possible as the required NA exceeds the theoretical limit of 1.44. There are three main avenues explored for extension of lithography to 32nm half pitch :

1) continue to increase NA at 193 nm beyond water limit using high index fluids and glasses (3); or
2) keep NA and wavelength the same, but go to lower k_1 through the use of double patterning (4); or
3) shorten the wavelength to 13.5 nm, in the extreme ultraviolet (EUV) (5).

Increasing NA further through the use of high index immersion fluids and glasses attracts much attention due to its promise for re-use of many infrastructure elements already in place for 193nm lithography, including reticles and laser sources. However, the development of new glass materials which meet all the optical requirements in addition to higher refractive index has many technical and economic difficulties, and suitable quantities are not expected before 2010. This does not meet the timeline of advanced customers, especially in NAND flash.

The second option, lowering effective k_1 through the use of double patterning, is also attractive from the point of view of infrastructure re-use. In this scheme, chip patterns so dense they are beyond the Rayleigh limit of k_1 0.25 are split into two or more less dense mask patterns, each with $k_1 > 0.25$. In an implementation, mask 1 is exposed and etched into a hardmask film. The wafer is then coated with resist and mask 2 is aligned to the etched pattern, exposed, then etched again. In this way, pattern resolution below the Rayleigh limit can be achieved. While promising the possibility of extending 193nm immersion technology to below 40nm half pitch , double patterning has many technical and economic challenges. The chief amongst these are required pattern to pattern overlay, and cost impact of doubling the number of critical patterning steps and mask count.

An interesting variant of double patterning uses spacer technology to form self-aligned structures at sub-resolution feature size (6). Spacer technology relaxes the requirements for tool overlay and mask registration errors, but requires even finer CD control, and significantly increases the number of deposition and etch steps required.. Cycle time through the fab will increase for all versions of double patterning compared to single exposure lithography.

Given realistic budgets for dose, focus, and overlay errors, double patterning at 193nm has a practical limit for resolution of approximately 22nm for one dimensional periodic structures such as in NAND devices and 29nm for two dimensional dense devices such as DRAM (7).

Wavelength reduction is the third option. Lithography has progressed for 30 years partly due to wavelength reduction, transitioning from 436 to 365 to 248 and now to 193 nm. Normally, wavelength changes take multiple tool generations to become mainstream technology – the industry needs several cycles of learning in order to integrate mask, tool, and resist. 193 nm has only now become the leading edge after 4 generations of tools. A shift to 157 nm was not successful due to, among other things, unavailability of CaF_2 crystals of satisfactory quality to produce projection lenses. Enormous resist and materials process integration issues (including mask and pellicles) are required. Refractive optics below 157 nm are not possible due to lack of suitable glass materials. Reflective optics are possible but are more complicated to fabricate. They are only beneficial if the wavelength reduction is sufficient to circumvent NA and k_1 limitations. EUV wavelength at 13.5 nm is about 15X shorter than 193 nm, allowing significant relaxation in NA and k_1, and offering several generations of further resolution extension, if other technical and economic challenges can be met.

Scanner tool introduction from ASML is paced by the shrink roadmaps of IC makers. The half pitch resolution, calculated at both k_1 0.27 (corresponding to NAND) and 0.4 (logic), offered by the last several tools is plotted versus date of product introduction in Figure 4. IC makers typically require 18 to 24 months from the receipt of the first tool to develop a process and ramp production. Figure 4 indicates that, while tool introduction schedules have been and will be on time for logic nodes at 65, 45, and 32nm (with corresponding half pitches of 90, 65, and 45nm), there is a serious problem meeting the timelines for NAND flash. As a result, double patterning is required to bridge the gap between single exposure water immersion lithography and EUV. Pre-production EUV tools are scheduled to be introduced in 2009.

4. Limits of Single Exposure, Double Exposure, and Double Patterning

It is useful to clarify the differences between single exposure, double exposure, and double patterning. Lithography in chip manufacturing generally uses a single mask exposure per layer. Here we define a Single Exposure (SE) as one exposure in which wafer stays in the scanner for the full exposure, with one resist spin and one develop. In this case, the Rayleigh resolution holds and k_1 is limited to 0.25 or higher. We define Double Exposure (DE) as two exposures, in which the wafer stays in the scanner for both exposures, with one resist spin and one develop. An example is the use of double dipole lithography (11). Here the Rayleigh limit also holds and $k_1 > 0.25$.

In double patterning (DP), the wafer is exposed with mask 1, leaves scanner for processing (e.g. develop, etch, first resist is stripped, second resist layer is spun on), then the wafer exposed with a second mask, developed, and etched. The effective k_1 can be less than 0.25, as illustrated in Figure 5 for the case of two masks with 3:1 lines and spaces, shifted by pitch/2.

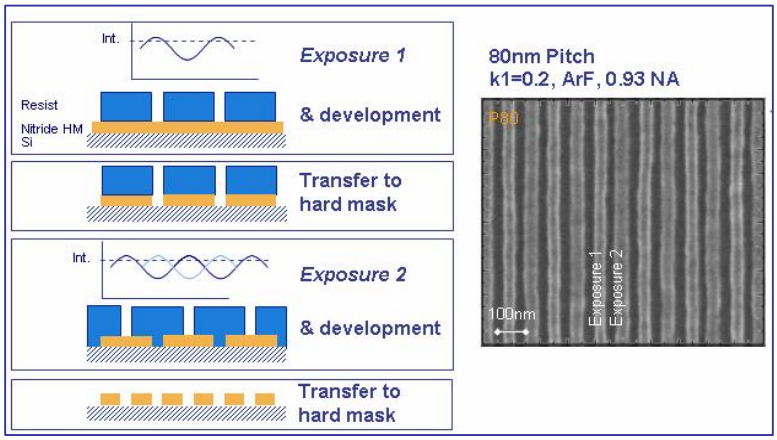

Figure 5: Double Patterning: a method to break the 0.25 barrier

In one dimensional imaging of simple lines and spaces, double patterning of two interdigitated gratings both at the Rayleigh limit forms a final composite pattern with half the Rayleigh limit, effective k_1 of 0.125. In theory, the limit of n separate patterning steps, the effective limit is $k_1 = 0.25/n$. In a practical sense it is not possible to infinitely subdivide images due to finite errors in mask, CD control, and overlay error. In two dimensional double patterning, the effective k_1 limit is $0.25/\sqrt{2} = 0.177$, and $0.25/\sqrt{n}$ for n patterning steps.

In double exposure, it is theoretically possible to image 2D patterns such as dense contact holes with crosspole illumination down to the k_1 0.25 limit. However, in practice, due to the significant zero order contribution and finite resist contrast requirements, quasar type illumination is the optimum choice, and k_1 is limited to 0.354.

The 1D and 2D limits of k_1 for SE, DE, DP, triple patterning and quadruple patterning are shown graphically in Figure 6. The theoretical limits are exact, while the practical limits shown correspond to curves assuming reasonable budgets for dose, focus, and mask errors. These curves would shift toward or away from the theoretical curves depending on these assumptions.

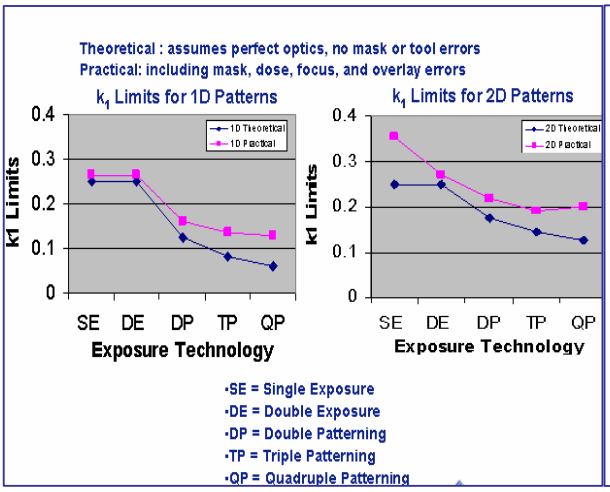

Figure 6: k_1 Limits for 1D and 2D Patterns

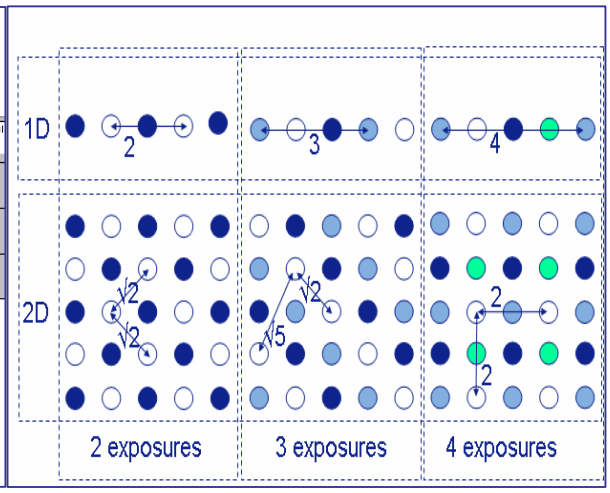

Figure 6a:Double exposure works best for 1D structures

In summary, single exposure theoretical limits are k_1 0.25 for 1D and 2D structures, but in practice k_1 is limited to ~0.35 for dense 2D structures. Double exposure techniques (e.g., DDL) can help to push closer to k_1 0.25 for dense 2D. Double patterning limits are k_1 0.125 and 0.177 for dense 1D and 2D features. With practical error budgets for dose, focus, overlay, etc. these are closer to ~0.14 and ~0.2 (20nm and 29nm HP at 193nm and NA 1.35). See Figure 7 for an example of ID patterning close to the practical limit. CDU budgets for double patterning are heavily dependent on the polarity of the process used, the overlay of the exposure tool, reticle CDU and misregistration, and LER.

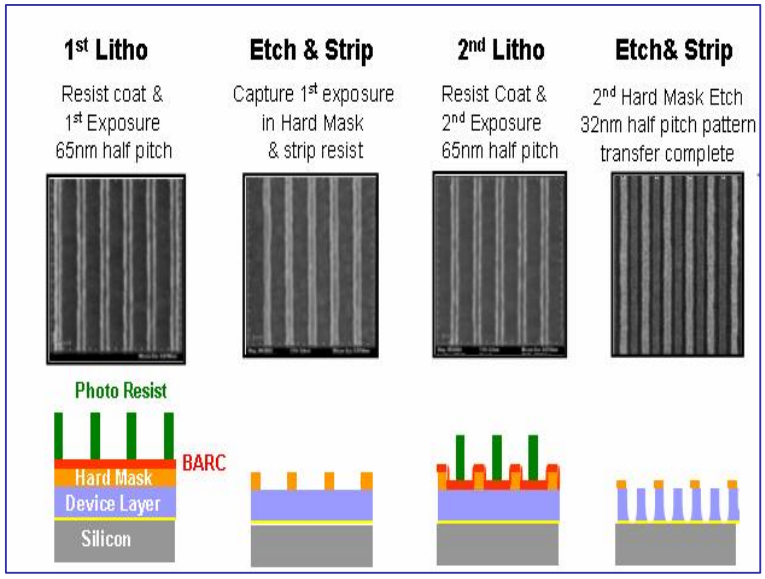

Figure 7: 32nm 0.85 NA ArF Double Patterning (k1 = 0.14)

5. Error Budgets for Single Exposure and Etch, Double Patterning and Spacer Double Patterning

In a single photo and etch step, the CD is determined by two error components, one from lithography and one from the etch (Figure 8).

In litho double patterning, where the first litho step is followed by an etch, then realigned, and etched again, one line edge is defined by patterning step 1, the other edge by patterning step 2. In order to account for the CD of each patterning step in the final pattern, we need to consider 4 adjacent edges, and define the final pattern CD by the position of its edges. By defining the CD from its edges, the CDU calculation includes both CD and placement errors (Figure 9).

In spacer double patterning, the CD is determined by a combination of errors from lithography, from deposition, from planarization, and from etch (Figure 10).

More on the error budgets for double patterning can be found in (13).

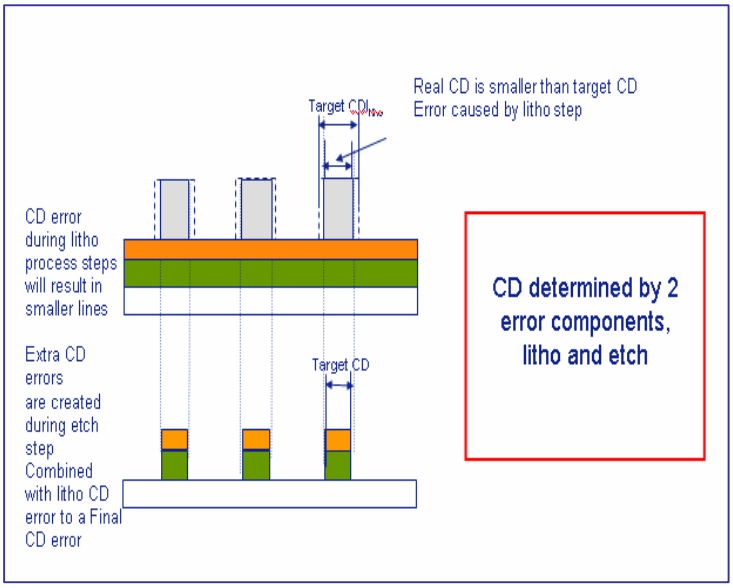

Figure 8:Single exposure patterning and CDU budget assumptions

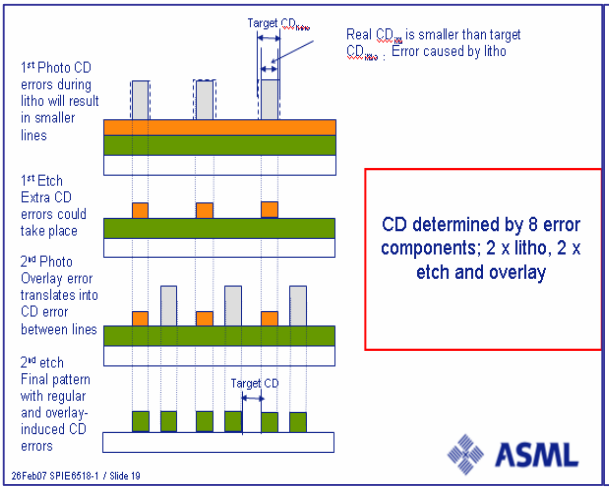

Figure 9: CD & Overlay for Double Patterning

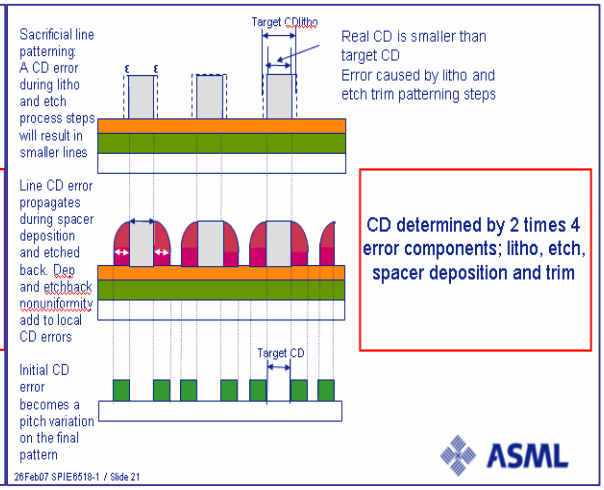

Figure 10: CD & Overlay for Spacer DPT

6. Metrology Requirements

Metrology for CD and overlay for high k_1 lithography is usually done in stand alone tools after the wafer is exposed and developed. A further CD measurement is taken after etch. This data is then fed into the factory APC system and may be used to adjust dose or overlay offsets for wafer lots which follow. This classical scheme is illustrated in Figure 11.

With the advent of low k_1 lithography, the process windows get smaller. Resolution enhancement techniques and optical proximity correction are used to improve image contrast and CD uniformity over the full range of feature types and sizes, requiring significant work in the reticle design and data preparation stages. Computational lithography is now a key technology employed before the wafer ever arrives at the scanner. Once the wafer comes to the lithocell the demand

for faster feedback is driving the incorporation of in-situ measurement tools for CD and overlay. This is illustrated in Figure 12. Table 1 indicates the evolution of sampling techniques, integration of metrology within the yellow room, optimization inputs for CD and overlay, as well as possible adjustments based on this data.

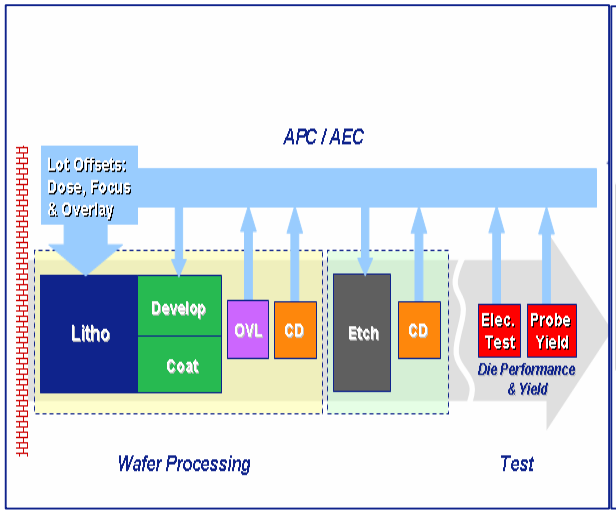

Figure 11: High k_1 Lithography Metrology & Process Control

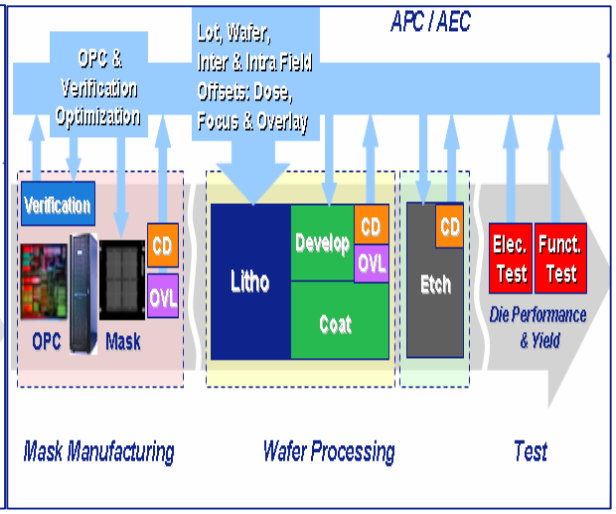

Figure 12: Low k_1 Lithography Metrology & Process Control

	Historical >130nm k_1>0.5	Current 130~65nm k1~0.4	Future < 65nm k_1>0.5	Future <45nm K_1~0.25 DE
Typical Metrology Sampling	Lot: ≥ 3 wafers Wafer: ≥ 5 points Die : 1 point	Lot: ≥ 5 wafers Wafer: ≥ 12 points Die : ≥ 1 point	Lot: All wafers Wafer: ≥ 25 Die : ≥ 4 points	Lot: All wafers Wafer: ≥ 25 Die : ≥ 4 points
Metrology Integration	Stand Alone Manual Corrections	Stand alone APC & AEC	Standalone & Integrated APC & AEC	Standalone & Integrated APC & AEC
CD & Overlay Optimization Inputs	Process design rules Parametric & Yield Results	Historical plus: Individual Mask, Equipment & Process step data	Current plus: Design / Design Hot Spots	SE Current plus: Film thickness in patterned area Input step 1 results into step 2 patterning
CD & Overlay Adjustments	Lot	Wafer global	Wafer local & Exposure Field	Wafer local & Exposure Field separate adjustments for each patterning step

Table 1: Evolution in Litho Metrology & Process Control

What's new for metrology in double patterning? Much tighter CD and overlay control is required, so that the metrology error is also challenged. As we have seen in the previous section, there is an entanglement of CD and overlay due to the formation of adjacent feature edges in separate patterning steps. Reticle registration is much tighter. Finally, in a spacer approach, the film thickness and conformality become part of the CD budget.

There are several possible approaches to take to meet these challenges. We can measure CD and overlay errors more representative of the true critical features through in chip CD and overlay measurements (Design Driven Metrology – (9)). Combined overlay and CD structures, at the critical feature size, can be devised and measured.

Double patterning always creates two populations, and metrology has to measure and differentiate both. Reticle CDU spatial fingerprint should be matched and reticle Mean-to-Target should be as close as possible. There is increased emphasis on active compensation to allow adjustment of pattern 2 based on the results of pattern 1.

In any litho double patterning scheme, overlay error becomes part of the CD budget. Overlay and CD cannot be treated anymore as separate measurements. As overlay errors impact CDU, it is important to measure overlay at resolution. At resolution features are more sensitive to image formation disturbances than traditional image-based overlay marks. This implies new types of overlay marks are needed. When using SEM CD metrology for overlay, an *anchor* is needed to measure image shift of the "at-resolution" target. See Figure 13 for the concept of a SEM target developed jointly with AMAT (12).

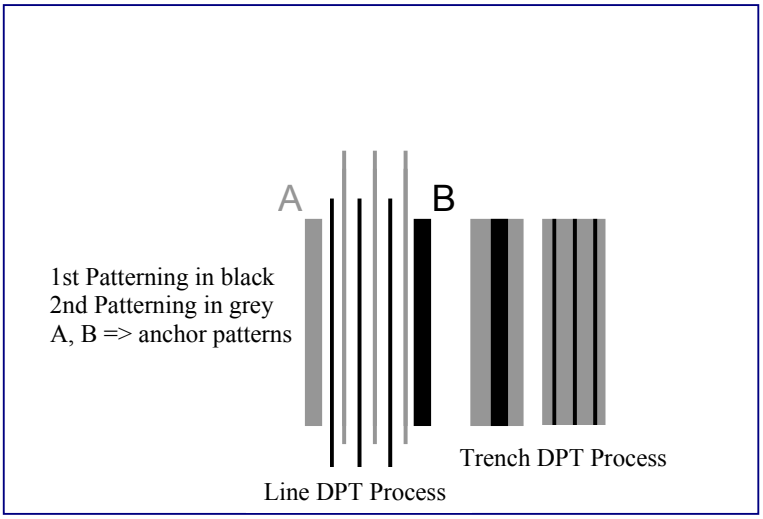

Figure 13: CD-SEM Overlay Principle: "COG" algorithm. Measure the Center of Gravity: distance between the absolute center of a measurement box and the center of the median feature within it (12).

Optimization of data sampling can lead to efficient ways to collect high quality CD and overlay data. See Figures 14 and 15 for illustrations of this from a scatterometry example. This will be important to collect enough data in a short amount of time as required for double exposure and double patterning.

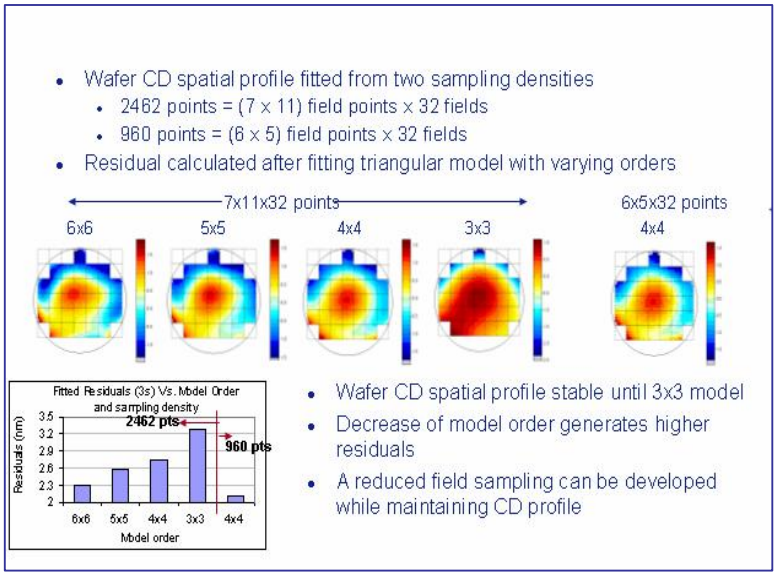

Figure 14: Sampling considerations: Changes in WaferInterfield

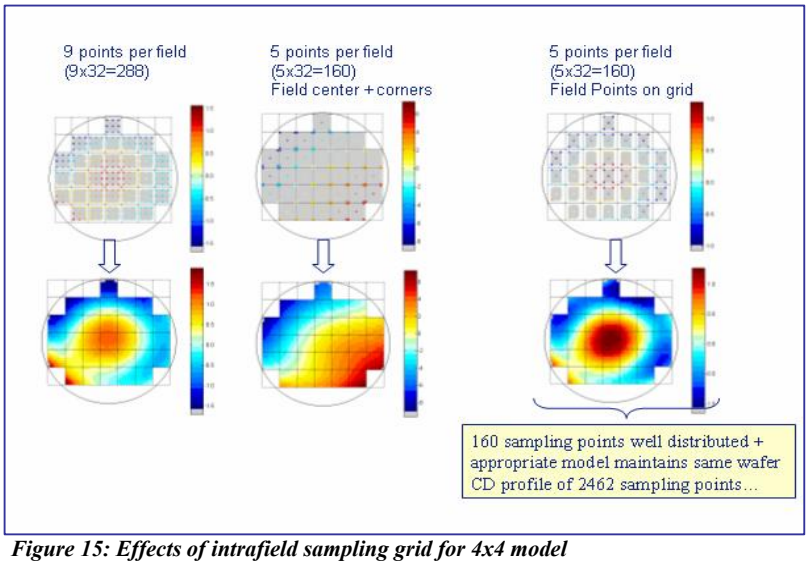

Figure 15: Effects of intrafield sampling grid for 4x4 model

7. Active compensation schemes

More, high quality data acquired while the wafer is still between patterning steps increases the value of active compensation to allow adjustment of exposure 2 based on the results of exposure 1. Dose can be adjusted to compensate for CD variations (DoseMapper principle – (8)). Likewise, overlay offsets can be introduced to compensate for correctable errors which are measured between exposure 1 and 2. See Figures 16 and 17.

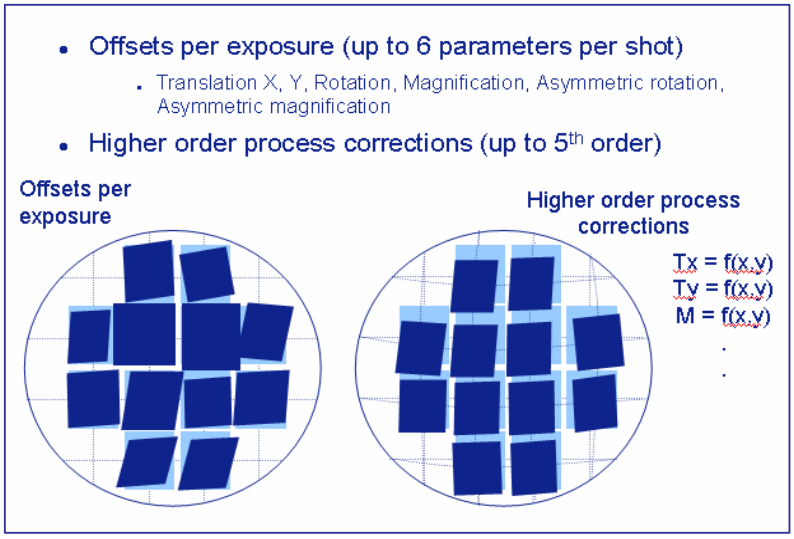

Figure 16: GridMapper – correction methods

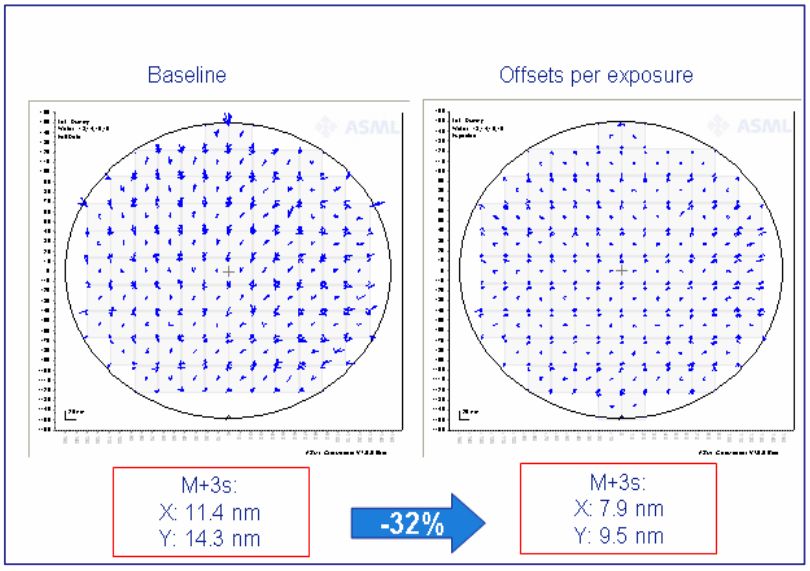

Figure 17: Using overlay offsets per exposure, an example from an 80nm DRAM process

With overlay error compensation (GridMapper principle), we can make offsets per exposure (up to 6 parameters per shot): translation X, Y, rotation, magnification, asymmetric rotation, and asymmetric magnification. The stepping grid can be adjusted with higher order process corrections (up to 5th order).

Feedback loops from in-situ CD and overlay metrology in the litho cell can be used for input to active compensation for double exposure. Likewise input from CD metrology in the etch tool can be used for active compensation in double patterning (Figure 18).

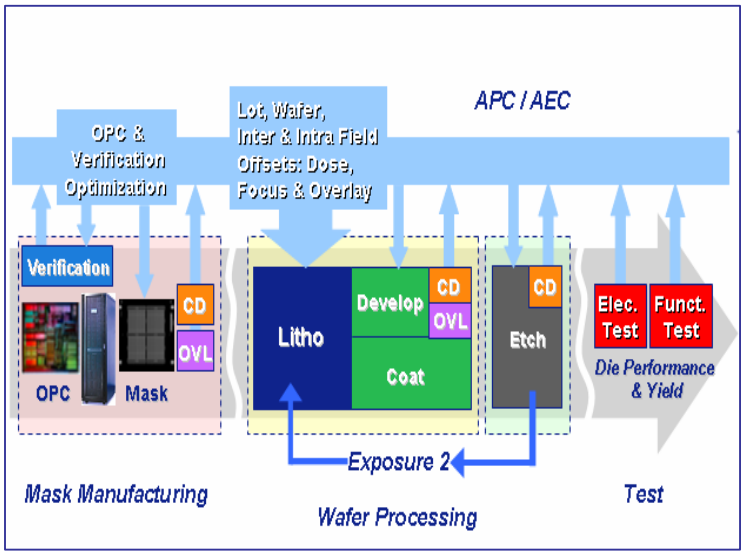

Figure 18: Low k1 Lithography Metrology & Process Control: with Double Patterning (Photo-Etch-Photo-Etch)

8. Conclusions

IC makers continue to demand further shrinks in order to reduce die cost. NAND flash devices lead the roadmap in shrink rate and timing. Lithography continues to be the main driver of the shrink. 193nm water immersion at NA 1.35 is capable of imaging 40nm half pitch. Resolution enhancement technology, RET, such as phase shift masks in combination with customized illumination and system optimization, is required to make the shrink producible.

Double exposure and double patterning solutions are being pursued to reduce effective k_1 below 0.3, and with required overlay and productivity. This is the only technology available for volume manufacturing in the 2008-09 timeframe. Realistic error budgets indicate double patterning is limited to about 29nm half pitch for complex IC patterns.

New challenges for IC metrology include the entanglement of CD and overlay errors and the need to distinguish the different populations. The need for rapid acquisition of high quality metrology data to support the unique opportunity to make corrections between patterning steps has also been explored.

8.1 Acknowledgements

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