# Advanced plasma etch technologies for nanopatterning

Rich Wise

IBM Semiconductor Research and Development Center, 2070 Route 52, Hopewell Junction, NY 12533

## ABSTRACT

Advances in patterning techniques have enabled the extension of immersion lithography from 65/45nm through 14/10nm device technologies. A key to this increase in patterning capability has been innovation in the subsequent dry plasma etch processing steps. Multiple exposure techniques such as litho-etch-litho-etch, sidewall image transfer, line/cut mask and self-aligned structures have been implemented to solution required device scaling. Advances in dry plasma etch process control, across wafer uniformity and etch selectivity to both masking materials and have enabled adoption of vertical devices and thin film scaling for increased device performance at a given pitch. Plasma etch processes such as trilayer etches, aggressive CD shrink techniques, and the extension of resist trim processes have increased the attainable device dimensions at a given imaging capability. Precise control of the plasma etch parameters affecting across design variation, defectivity, profile stability within wafer, within lot, and across tools have been successfully implemented to provide manufacturable patterning technology solutions. IBM has addressed these patterning challenges through an integrated Total Patterning Solutions team to provide seamless and synergistic patterning processes to device and integration internal customers. This paper will discuss these challenges and the innovative plasma etch solutions pioneered by IBM and our alliance partners.

**Keywords**: plasma etch, sidewall image transfer, atomic layer etch, surface integrity, defectivity

## DISCUSSION

The relentless demand for ever increasing semiconductor capability has driven a technology revolution in non-equilibrium plasma processing. The anisotropic pattern transfer from lithographically defined resist patterns into the thin films of semiconductor devices requires continual improvement in pattern fidelity, thru-pitch pattern control, uniformity within each wafer and process window across incoming variations. As fundamental limits in imaging integrity and physics of the underlying devices are approached, novel plasma based pattern transfer techniques have been introduced to continue the device performance roadmap.

IBM has a long history of leadership in technology innovation (Fig 1.), enabled by advances in patterning and pattern transfer. The pace of these technology innovations has accelerated as we approach the end of optical lithography scaling. 3 dimensional structures (e.g. FinFET), silicon nanowires, EUV lithography, and directed self-assembly techniques are just a few of the candidates for incorporation over the next several technology nodes, each requiring revolutionary innovation of plasma based pattern transfer techniques.

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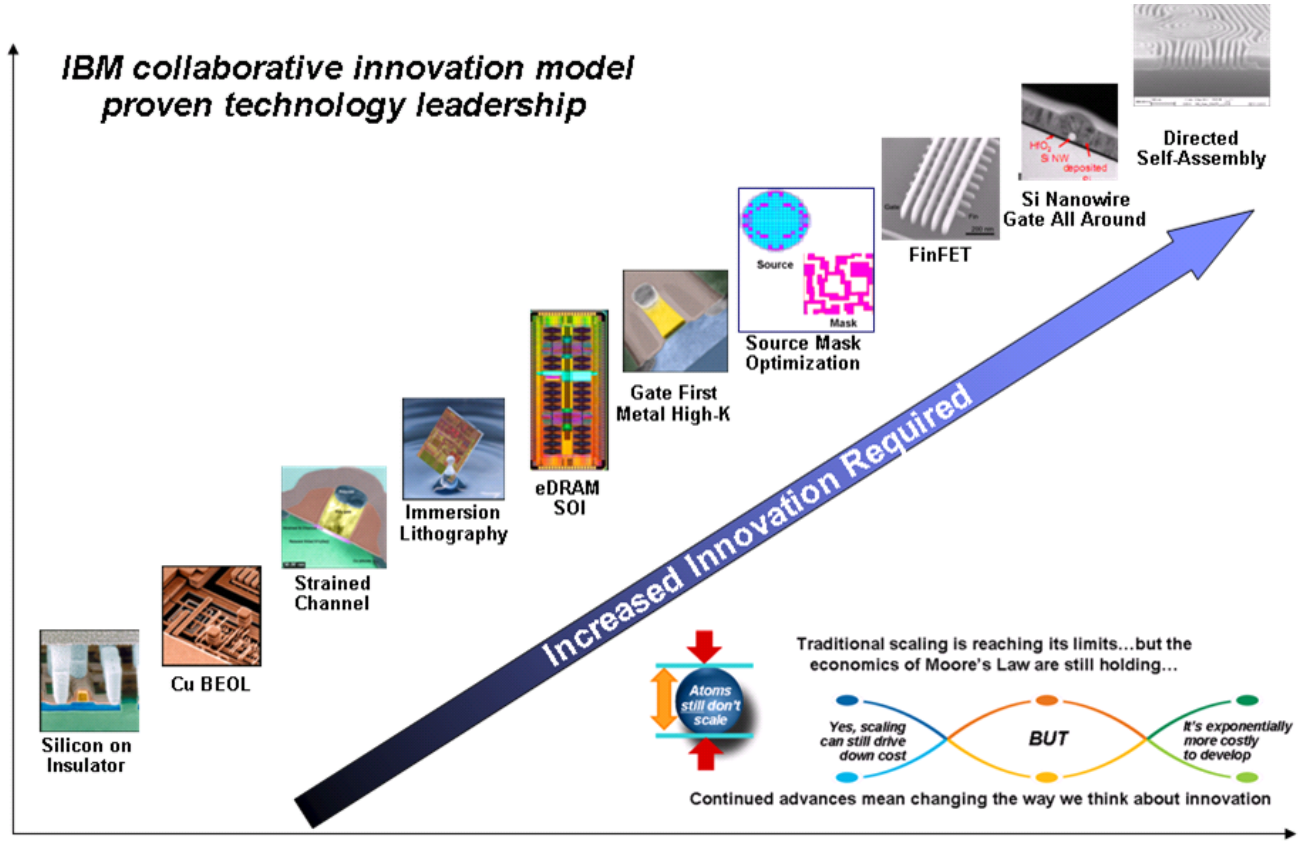


Figure 1. IBM Semiconductor Technology Innovation Roadmap

Plasma etch for critical dimension shrink is a well established technique to deliver sub minimum gate length and contact/via size. A heavily polymerizing chemistry is applied to taper sacrificial films and reduce the final feature size. The overall degree of shrink and consequent polymerization level has continued to increase as the difference between image size and final design pattern size has increased (Fig. 2). Management of this polymerization requires a high level of control of exposed surfaces in the plasma etch reactor to prevent excessive accumulation of deposition byproducts and resultant defectivity. Plasma etch processes and equipment must manage this polymerization across mask features, in particular large features tend to exhibit inverse RIE lag, potential for etch stop, and through pitch CD variation. Novel plasma processing techniques are being developed that integrate heavily depositing processes (RIE lag) with lean processes (inverse RIE lag), typically by gas or RF pulsing. These techniques have been shown to be effective in minimization of aspect ratio dependent etching (ARDE) and thru-pitch variations, but drive additional operating complexity, defectivity risk, and capital and operating costs[1].

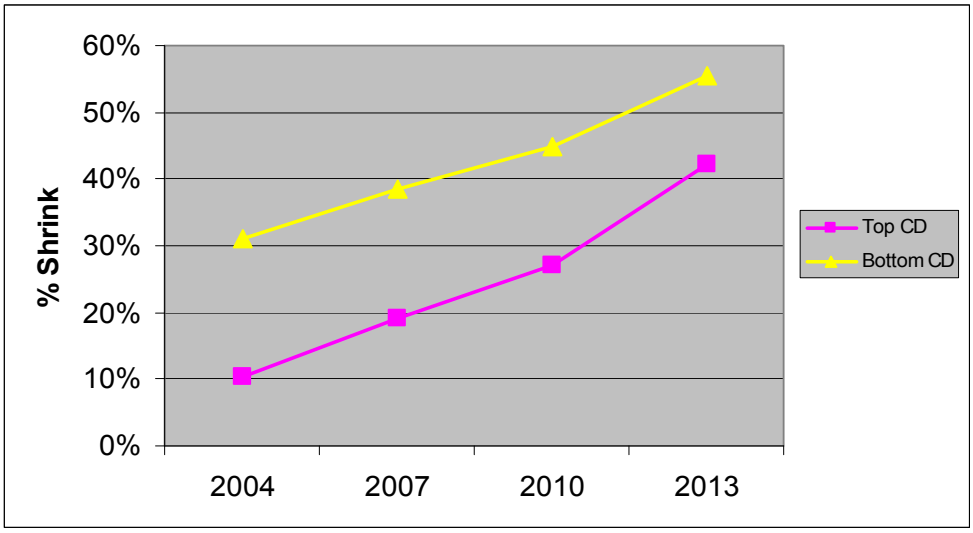


Figure 2. Contact CD Shrink Evolution for Immersion Lithography

Continued scaling in device density also requires sub-minimum pitch resolution (Fig 3.). Common solutions employed to enable sub-minimum pitch devices are double (or multiple) patterning and sidewall image transfer. Multiple patterning uses multiple exposures to split the pitch between the multiple exposure or to define a cut mask which defines orthogonal separation between features[2]. These multiple exposures also allow for corrective imaging techniques such as printing resolution assist features (pRAF) to be used to further extend imaging capability. Mulitple patterning typically requires additional plasma etch patterning steps to memorize the first exposure into an underlying film, as well as additional etch patterning step to open the planarizing film used in (at a minimum) the second imaging pass.

Sidewall image transfer (SIT) uses a sacrificial mandrel to define a spacer on two sides of the mandrel line, the spacers are then used as a mask to double the pitch frequency. SIT requires additional spacer definition plasma etch processes and mandrel removal steps. Precise control of the spacer shape is required to prevent CD variation across devices, and variability in the mandel critical dimension can result in pitch variability. High selectivity may be required during the mandrel removal or spacer etch processes depending on the integration employed to define films below.

However defined, pitch scaling will decrease the process window for shorting between vias and lines. The overlay capability of existing imaging lithography becomes problematic as the half-pitch approaches the desired via size, particularly for the contact module between wiring levels to the device source and drain, when isolation of contact from gates is critical. Self-aligned structures at via and contact levels allow for relaxed overlay requirements but require the ability to selectively stop on exposed corners. High sputter yield at exposed corners requires precise management of the ion energy distribution and flux[3], and high level of passivation requires careful management of deposition to prevent etch stop and degraded opens yield. Self-aligned structures may require more strongly decoupled source designs or pulsing of the deposition (by bias power or gas phase polymerization) to enhance deposition and minimize sputter damage of the isolation structures[4].

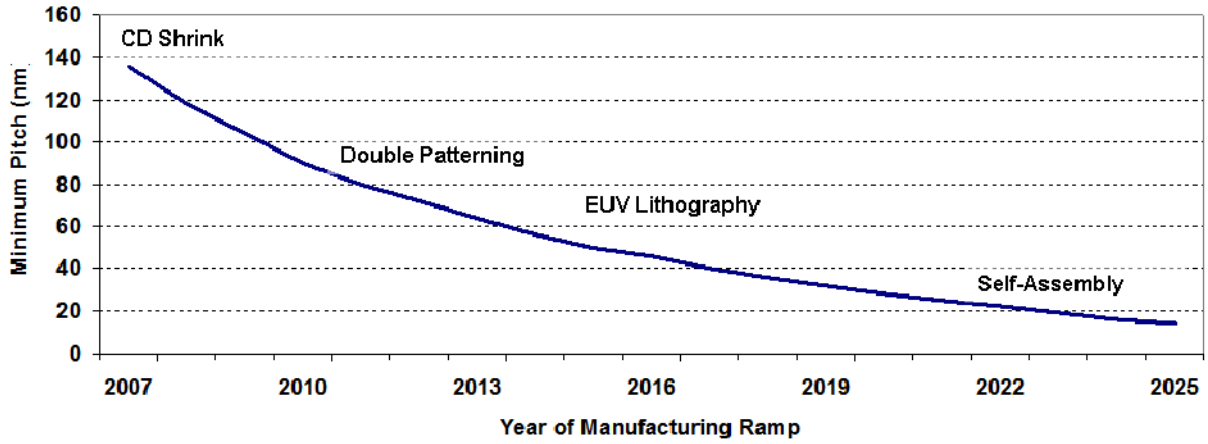


Figure 3. Pitch Scaling

Scaling of device architecture requires a continual step down in the budget for silicon consumption in the source drain region between gates[5] (Fig 4.). This region is exposed to multiple plasma processing steps, during implant mask strips, the overetch portions of spacer etch, the overetch portions of any liners to be removed, and during contact hole patterning steps. Increasingly complex device integration has resulted in an increase in the number of these plasma processing steps and subsequently reduced the silicon loss budget for each pass. This has hastened the migration to novel plasma equipment for control of the ion bombardment energy to reduce ion mixing and consequent silicon loss. Higher frequency bias power supplies (to reduce the bimodal ion energy tail[6]), more strongly decoupled plasma sources, plasma pulsing (to reduce ion flux[7]) and elevated temperature wafer processing equipment (increasing chemical reactivity) are being introduced at various stages to minimize the damage to underlying silicon. Atomic layer etch techniques are in exploration as a method to provide self-limited decoupling of plasma surface damage and surface reaction and desorption[8].

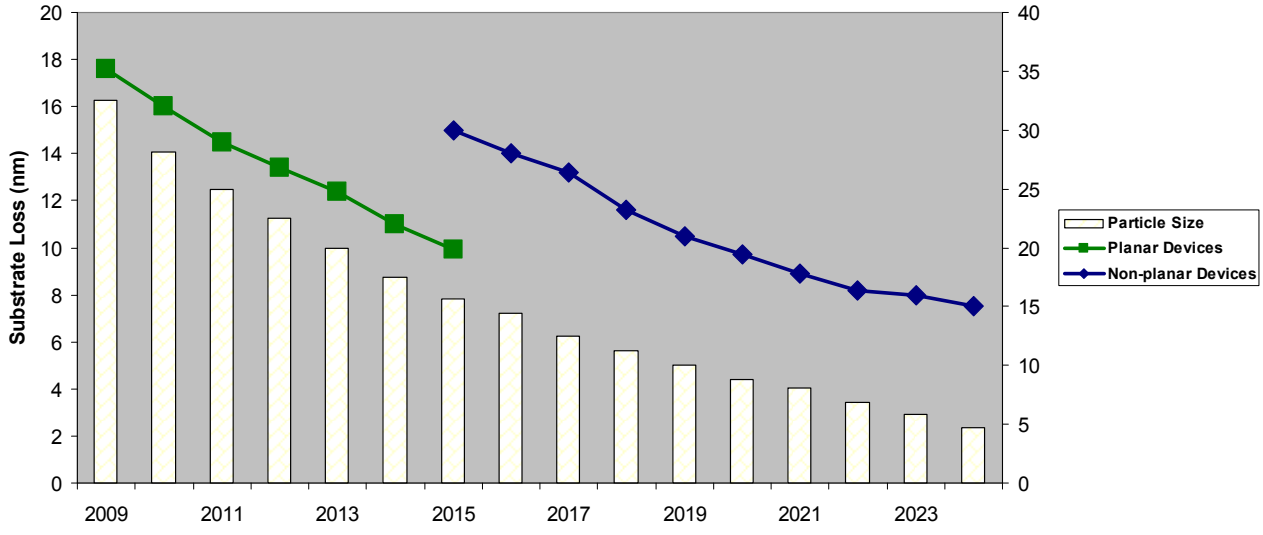


Figure 4. Substrate Budget and Defectivity Roadmap

The additional plasma etch challenges being introduced to continue scaling have resulted in a consequent increase in required plasma etch processing steps for each subsequent technology node, approximately 30% node-node (Fig 5.). In particular, the requirement for thinner substrate and etch stop layers has led to an expanded role for conductor etch equipment in the process flow. In many cases these levels may not have been considered a critical mask level (e.g. strained liner, spacer definitions, silicon recess etches) however they now drive a large portion of the source technology in the fabricator.

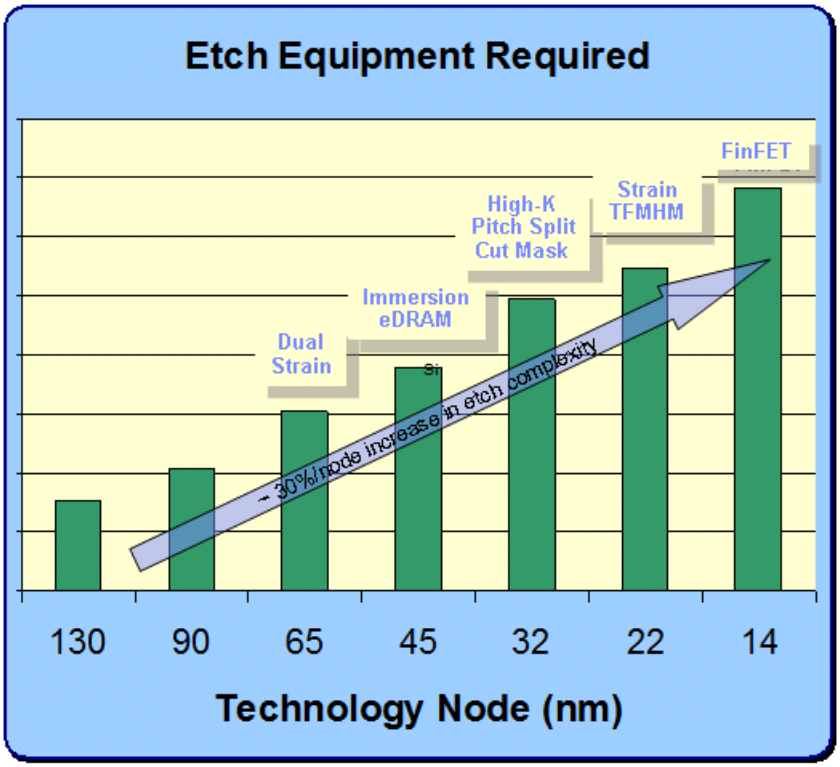


Figure 5. Plasma Etch Equipment Requirements

A key technical challenge for next generation plasma etch technology is a reduction in the inherent charge separation from non-equilibrium plasma sources (Fig 6.). This differential charging can result in feature distortion (long range line edge roughness), micro-trenching of feature bottoms, and irregular patterned high aspect ratio features. Charge separation becomes more critical on advanced technologies as the ion bombardment energy is reduced to minimize corner rounding or substrate damage. Temporal afterglow (e.g. source pulsing techniques) and spatial afterglow (e.g. larger plasma diffusion lengths between source and wafer) have been explored to reduce the level of charge separation in high aspect ratio features. Lower throughput will be a challenge for cost management, due to the reduced duty cycle of pulsing systems or larger diffusion path for spatial afterglow sources. Advanced techniques including ion-ion plasma and anisotropic neutral beam sources are in exploration and may be required as aspect ratio and substrate damage scaling continue[9]. These solutions will require a long term technology commitment by suppliers to become manufacturable solutions.

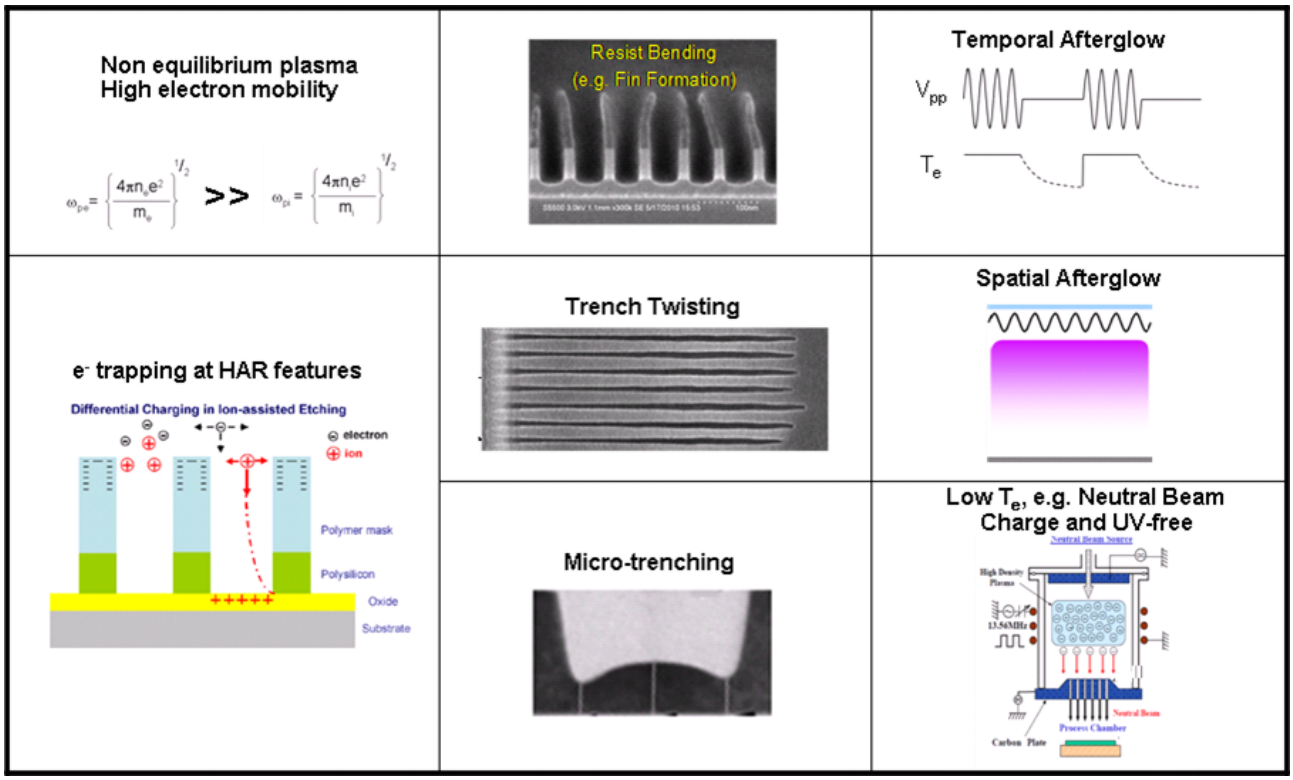


Figure 6. Non Equilibrium Plasma Charge Separation

Advanced plasma source design for improved surface integrity will require strict management of ion bombardment energy and the depositing species required for passivation (Fig 7). By employing elevated wafer temperatures and appropriate chemistry selection a low sticking coefficient and high sputter yield may be obtained to minimize the required ion energy (and surface mixing) for etching to proceed. This will minimize ion mixing and loss of stop layers or chamfer of exposed corners. Atomic layer etching will be required as scaling approaches the atomic scale, e.g. repeated cycles of absorb – activate – evacuate shown in ref 8.

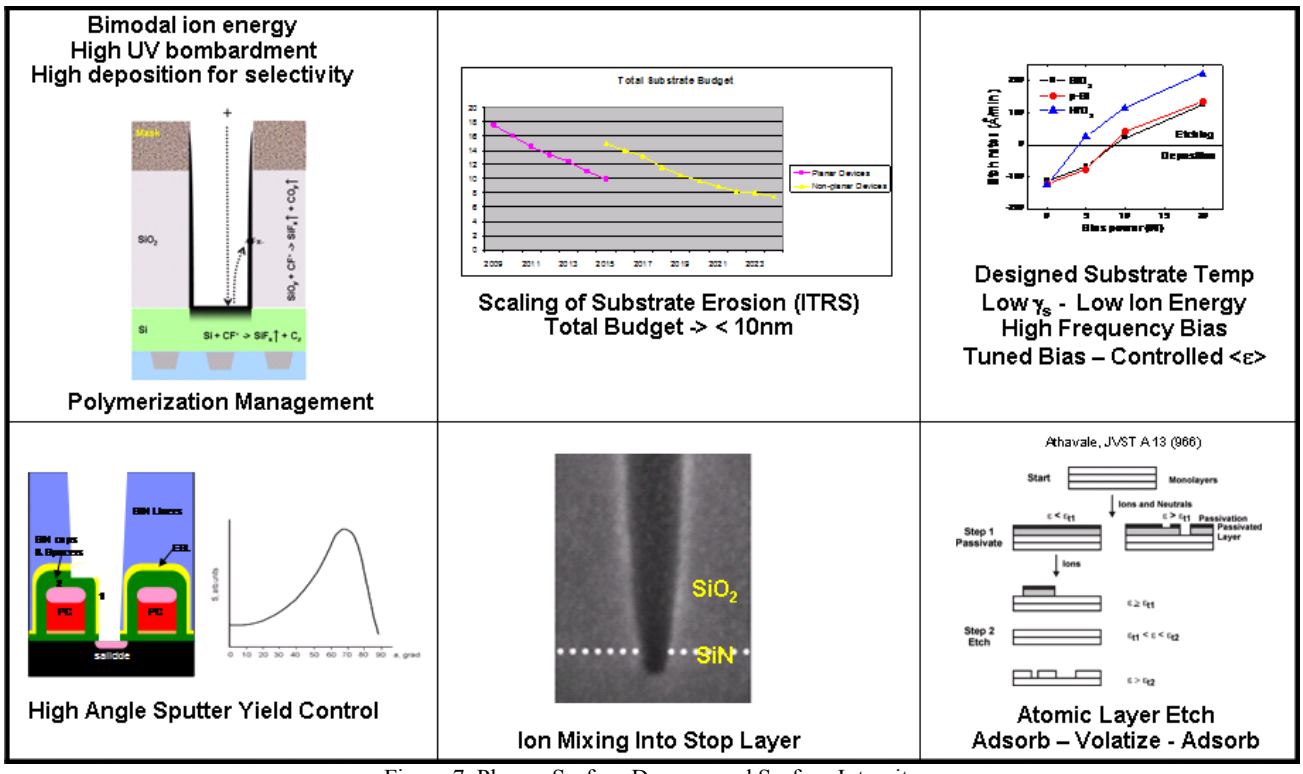


Figure 7. Plasma Surface Damage and Surface Integrity

Decreases in film thickness and tighter tolerances have resulted in a concurrent reduction in plasma process operating window and consequent need for improved plasma process uniformity across wafer. Highly flexible uniformity tuning on plasma etch equipment has become the norm, gas flow (flow weighting and additive gases), power, and wafer temperature are all regularly employed to adjust radial uniformity of the plasma operating chamber (Fig 8). Rapidly adjustable wafer pedestal temperatures are used to adjust wafer temperature and reaction/sticking coefficients during different steps of a given etch process, increasing flexibility for complex film stacks. Plasma volume may be varied to provide the optimum diffusion length and plasma flux to wafer. These parameters have provided a dramatic stepdown in cross wafer uniformity, and are on track to provide Angstrom level CD control cross wafer.

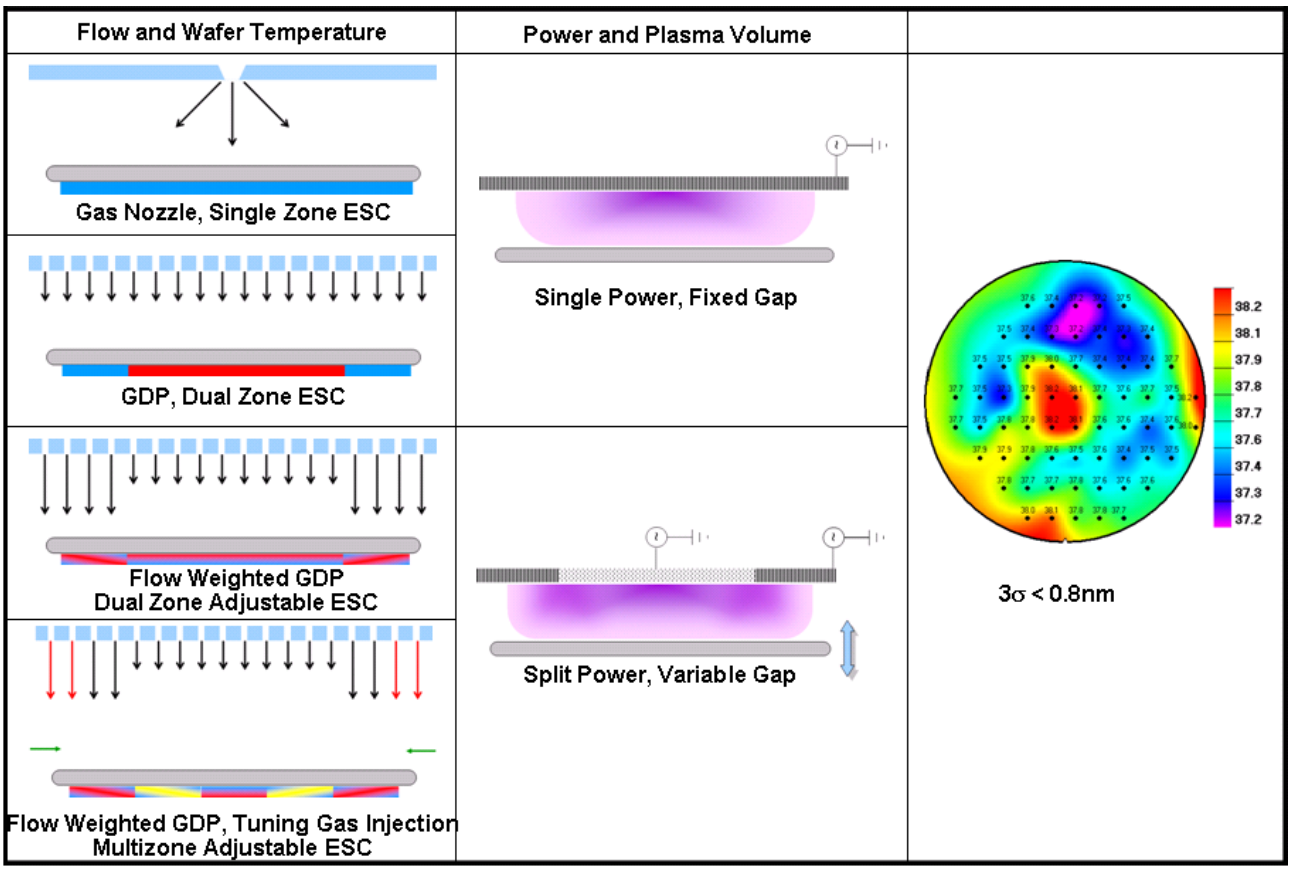


Figure 8. Plasma etch uniformity tuning

Acceptable plasma process defectivity scales with feature size, and smart operation of plasma etch equipment (e.g. continuous plasma, pre-coating techniques, $N_2$ purges) are required to meet these stringent targets. Discontinuities at the physical boundary of the wafer result in step changes in material loading, applied bias power and wafer edge temperatures (Fig. 9). Mechanical limitations of wafer handling require a physical gap at the wafer edge and surrounding apparatus. This mechanical gap is typically larger than the debye length of the plasma. Plasma penetration into this gap and elevated wafer temperature beyond the limit of He backside cooling may lead to elevated etch rate at the wafer bevel region, high levels of deposition in the gap between the wafer edge and surrounding apparatus, or both. Smart management of the materials and temperature of the surrounding equipment apparatus is required to meet reliability and yield targets.

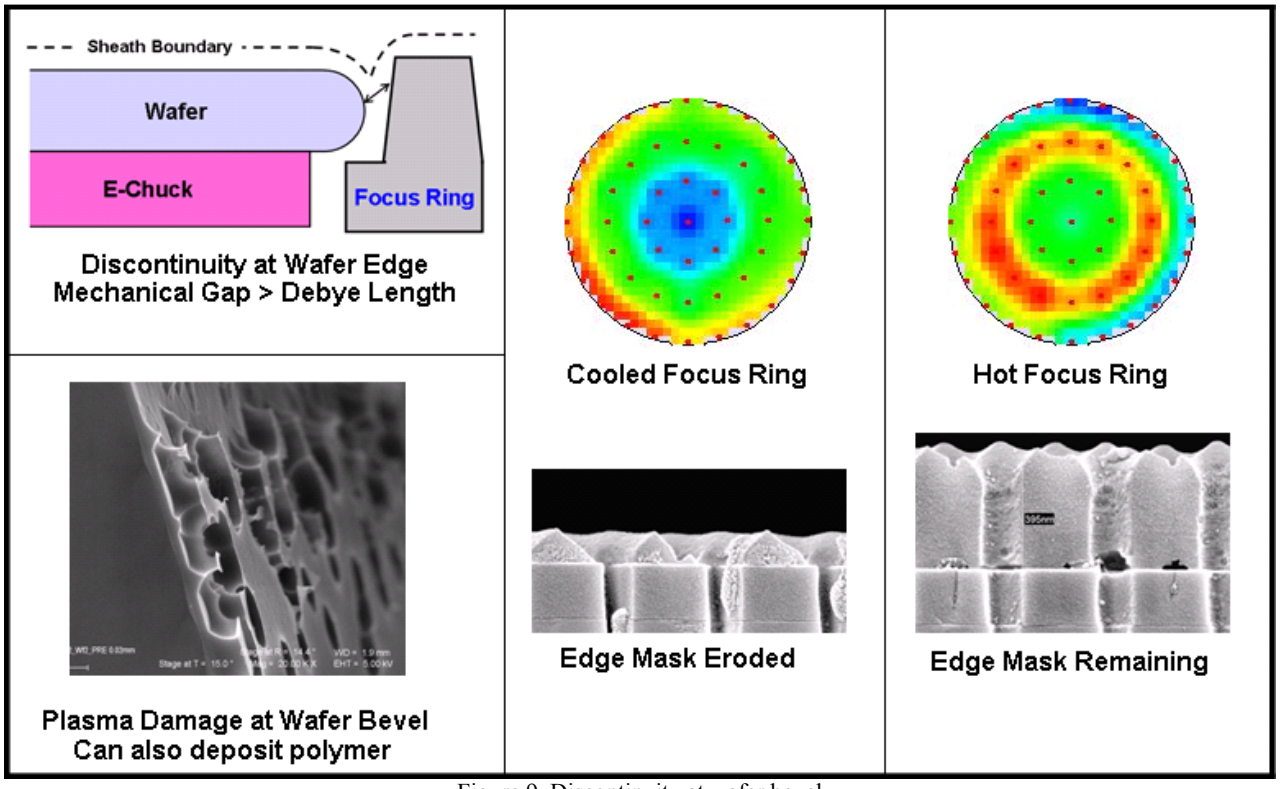

Figure 9. Discontinuity at wafer bevel

## SUMMARY

Scaling challenges in device pitch and vertical device integration have introduced new challenges to non-equilibrium plasma processing. Advanced techniques, such as multiple etch patterning, afterglow plasma processing, and atomic layer etch are being actively explored to meet these challenges. Continued improvement in manufacturability, particularly defectivity and uniformity, have been enabled by introduction of advanced plasma etch capabilities for tuning and polymer management. Integration of lithography and etch into a patterning solutions team has been key to enabling IBM technology roadmap.

## ACKNOWLEDGEMENTS

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