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Contact inspection and resistance–capacitance measurement of Si nanowire with SEM voltage contrast

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Abstract. A methodology to evaluate the electrical contact between nanowire (NW) and source/drain in NW FETs was investigated with SEM voltage contrast (VC). The electrical defects are robustly detected by VC. The validity of the inspection result was verified by transmission electron microscope (TEM) physical observations. Moreover, estimation of the parasitic resistance and capacitance was achieved from the quantitative analysis of VC images, which are acquired with different scan conditions of an electron beam (EB). A model considering the dynamics of EB-induced charging was proposed to calculate the VC. The resistance and capacitance can be determined by comparing the model-based VC with experimentally obtained VC. Quantitative estimation of resistance and capacitance would be valuable not only for more accurate inspection but also for identification of the defect point. [DOI: 10.1117/1.JMM.18.2.021205]

Keywords: critical dimension-scanning electron microscope; nanowire; voltage contrast; contact inspection; resistance measurement; capacitance measurement.

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1 Introduction

Si FinFET[1] is widely used for high-performance logic devices. It has overcome performance deterioration due to size scaling of Si planar FET. However, FinFET has its limit of scaling as well. Nanowire FET (NW FET) is one of the promising options for further scaling of logic devices. NW FET[2] would give better electrostatics than FinFET with scaled dimensions since short channel effect can be suppressed by the gate-all-around structure.

Fabrication process of NW FETs is more complex than that of FinFET. Figure 1 shows the overview of the typical process flow of NW FET.[3] The main differences from the FinFET process are the following two steps. The one is the epitaxial growth of stacked Si/SiGe layers [Fig. 1(b)]. The other is selective SiGe removal step to release NWs (NW release step) [Fig. 1(e)], which is inserted after dummy gate removal step.

The NW release step is the critical step in the NW FET fabrication. The released NWs are suspended over the gate trench and supported only by small area where NW is attached to source/drain (SD), as shown in Fig. 2. This contrasts with FinFET fabrication process, in which fins are stably standing on the Si substrate and supported by SD touching through all side areas of the fins. This means that the risk of mechanical defect is much more serious in NWs at NW–SD interface. The inspection of NW–SD contacts is therefore important. However, inspection of physical defects at the NW–SD interface is difficult by top-down inspection because the interface is concealed by the spacer above it. Alternatively, electrical defect inspection would be an option.

An electrical defect inspection method utilizing SEM voltage contrast (VC) is well-established as a nondestructive inline method. VC is an SEM signal contrast, which is caused by the surface potential difference. A floating pattern is charged by electron beam (EB) irradiation, and a grounded pattern is not charged. Thus, an electrical defect can be inspected by checking this charging condition difference by VC. A typical procedure of VC inspection consists of two separate EB irradiations, where the first one is for charging the surface positively and the second one is for signal detection to acquire an SEM image. However, this two-step procedure does not work if charge leak is faster than the interval between two irradiations. For such a case, one-step procedure is effective. Charging induced by the EB scan for image acquisition itself is detected simultaneously.

The mechanism of VC is shown in Fig. 3. Figure 3(a) is a schematic illustration of SEM signal detection from positively charged sample with an energy filter. The secondary electrons (SEs) can be classified into three energy regions. (1) SEs whose energy is lower than eV_S: they are trapped backed to the surface, (2) SEs whose energy is between eV_S and $eV_S + E_F$: they are filtered by energy filter, and (3) SEs whose energy is higher than $eV_S + E_F$: they can be detected by the detector. In other words, the threshold SE energy for signal detection is $eV_S + E_F$. Figures 3(b)–3(e) show the detected electrons in the SE spectrum. In case of no surface charging and without energy filtering, all SEs can be detected [Fig. 3(b)]. With charging, SEs whose energy is smaller than the surface potential eV_S cannot be detected [Fig. 3(c)]. When energy filter is applied and the sample is not charged, SEs whose energy is smaller than filtering energy E_F cannot be detected [Fig. 3(d)]. Finally, when the charged sample is observed with energy filtering, only SEs whose energy exceeds $eV_S + E_F$ can be detected. The difference between Figs. 3(b) and 3(c) corresponds to VC without energy filtering, and the difference between Figs. 3(d) and 3(e) corresponds to VC without energy

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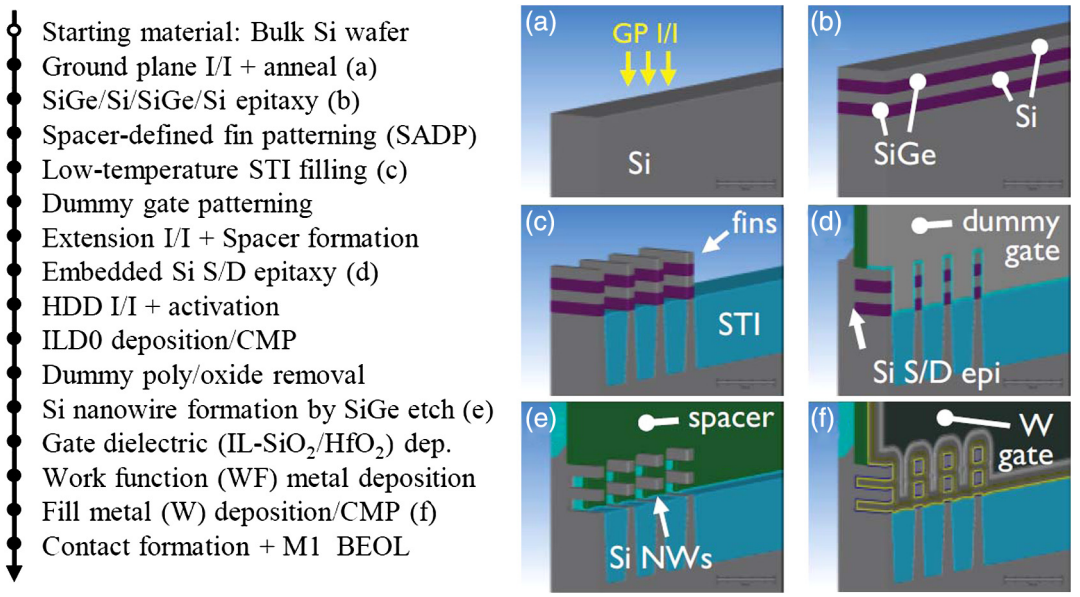

Fig. 1 Process flow of Si NW FETs fabrication.

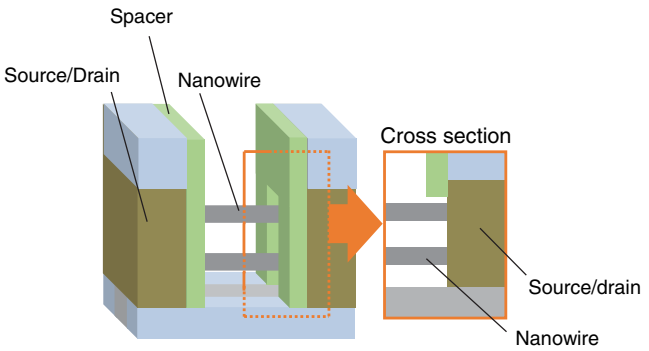

Fig. 2 Schematic configuration of NW FET and its cross-section parallel to the NW.

filtering. As shown in Fig. 3, VC is enhanced by energy filtering with appropriate threshold energy.

VC-based inspection is already established for local contact, gate-leak, and dynamic random access memory capacitor.[4–7] Failure mode classification was demonstrated by changing the scan direction of EB, considering the device circuit.[8] The VC method should be applicable to NW–SD contact inspection, although there is no experimental verification yet. This paper and our previous report[9] describe the validity of the VC-based NW–SD contact inspection.

Furthermore, it would be valuable if parasitic resistance (R) and capacitance (C) can be measured. Qualitatively, the impact of changing the scan direction of EB was discussed with an RC model.[7,8] It is already reported that rough estimation of parasitic resistance is only possible by evaluating VC.[10] Pulsed irradiation of EB by a special apparatus has been applied to analyze the charging dynamics, which gives information on both resistance and capacitance.[11] However, quantitative estimation of resistance and capacitance has not been realized by a conventional SEM with continuous EB irradiation. We propose an alternative approach to investigate and quantify the charging dynamics by continuous EB irradiation. Changing the scan speed is equivalent to changing the duration of continuous EB irradiation on single NW. The VC response should change when the duration time is exceeding the charging relaxation time (RC relaxation). Thus, a quantitative analysis on the VC images acquired with different scan speeds would enable the parasitic resistance and capacitance estimation. The feasibility of this approach for resistance and capacitance measurement of NWs FET was also investigated in this study.

2 Methods

2.1 *Sample and Measurement Conditions*

The inspected samples are suspended NWs, which were fabricated by stopping the NW FET process flow after the NW release step [Fig. 1(e)]. Two NWs are vertically stacked as shown in Fig. 2. Only top NWs were inspected since the experiment was performed by top-view SEM.

The design length of the NWs is 70 or 28 nm. The typical diameter of the NWs is 8 to 10 nm for both types. Figure 4(a) shows an example of a top-view SEM image of 70-nm-long NWs and Fig. 4(b) shows a tilted-view SEM image of the NWs fabricated by the same process. As defined in Fig. 4, x axis is parallel to NWs and y axis is perpendicular to NWs.

2.2 *Measurement Conditions*

All SEM images were taken with a critical dimension-scanning electron microscope (CD-SEM) (Hitachi CG6300). VC images discussed in this paper were obtained by the one-step procedure, in which sample charging and image acquisition are done by single EB scan simultaneously. This is because the two-step procedure gave no clear VC of the tested NWs regardless to the experimental condition.

This study consists of two experiments. One is verification of VC-based NW–SD contact inspection of NWs FET, that is, defect or nondefect test. The other is a feasibility study of R and C measurement of NWs FET.

The experimental conditions used in these two experiments are the following. For the NW–SD contact inspection,

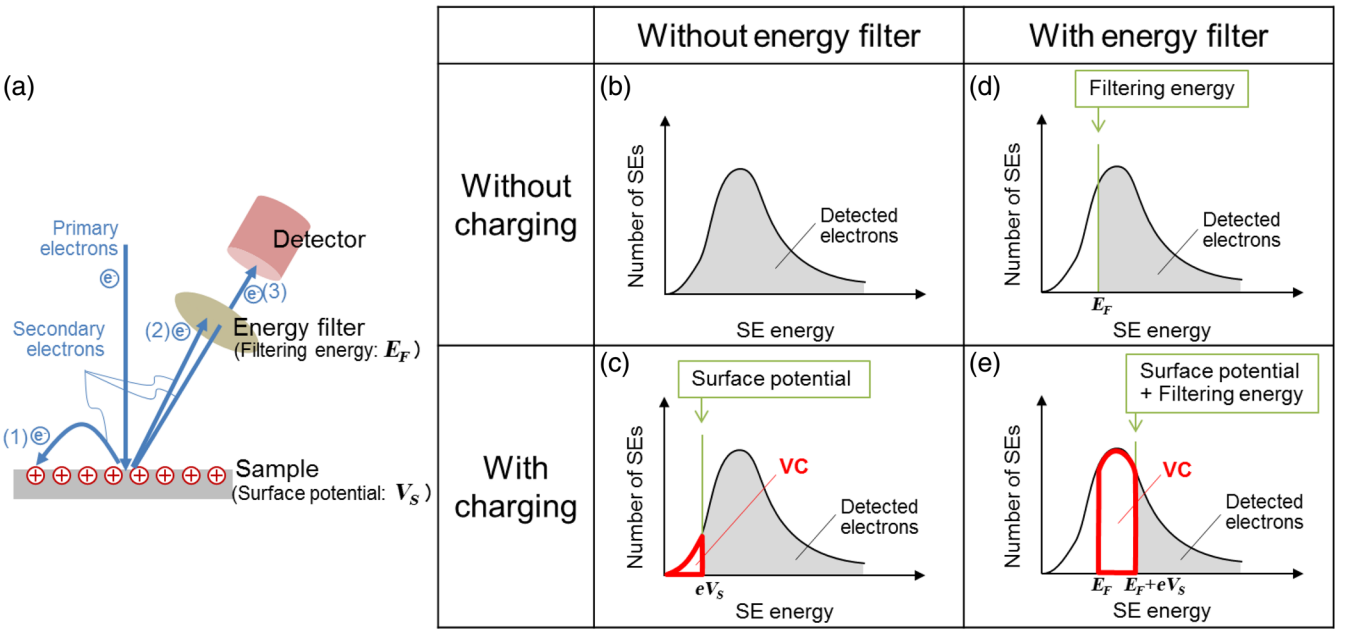

Fig. 3 (a) A schematic illustration of SEM signal detection from positively charged sample with an energy filter. SE spectrum (a) without charging and without an energy filter, (b) with charging and without an energy filter, (d) without charging and with an energy filter, and (e) with charging and with an energy filter. Shared area corresponds to the detectable electrons. Area surrounded by bold lines corresponds to VC. VC is enhanced by energy filtering.

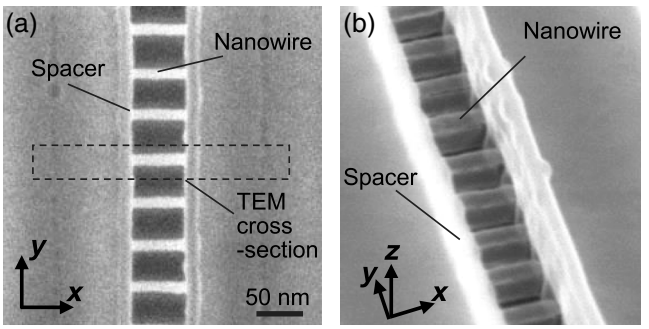

Fig. 4 An example of (a) top-view SEM image of the NW sample and (b) a tilted SEM image.

accelerating voltage was 800 V, probe current was 8 pA, number of frame integration is 32, field of view is 337.5 nm^2, scan speed is 6.6 mm/s, and pixel size is 0.66 nm. They are the typical conditions for CD-SEM measurements. The automatic brightness and contrast adjustment function were disabled to make the gray-level comparison possible. About 1680 NWs (70-nm long) were inspected across a wafer to discuss the statistics of the electrical defects.

As for the R and C measurement, two scan directions (along x and y axes) and three different scan speeds (53, 6.6, and 0.82 mm/s) were used. These three scan speeds are denoted hereafter by high-, middle-, and low-speed scans, respectively. Probe current was 100 pA in this experiment. Other experimental conditions are the same as those of the NW–SD inspection experiment. Since the size of field of view was fixed, the image acquisition takes shorter time for high-speed scan and longer time for low-speed scan. It means that the duration of continuous EB irradiation on a certain NW was changed. Thus, the charging dynamics can be investigated by comparing the VC results with different scan speeds.

Cross-sectional transmission electron microscope (TEM) images were obtained on a part of inspected NWs. The results of VC-based inspection of NW–SD contact were verified by comparing with the TEM results. The location of TEM observation was shown by the dashed line in Fig. 4(a). About 10 NWs (70-nm long) and 6 NWs (28-nm long) were inspected by both VC and TEM.

2.3 *Model for Quantitative Voltage Contrast Analysis*

A model to calculate VC was proposed. As mentioned in Sec. 2.2, VC was not observed by two-step procedure though it was observed by one-step procedure. It suggests that the discharging of a top NW happened in short-time scale comparable to the scan time scale. To express this dynamic of charging and discharging during EB scan, RC relaxation was introduced in the model. The input parameters of the model are EB conditions (accelerating voltage, probe current, scan speed, and threshold energy of energy filtering), specimen dimensions (top NW diameter in this case), and electrical conditions of top NW (parasitic resistance, R, and capacitance, C). Its output is the detected SEM signal, namely, VC. Among the input parameters, only R and C are the floating parameters since other parameters are given ones. Thus, R and C can be determined by finding the best parameters to reproduce the experimentally obtained VC.

The model consists of three steps, as shown in Fig. 5. The first step [Fig. 5(a)] is to calculate the injected current into the top NW, I, by Monte Carlo simulation.[12] Monte Carlo simulation is usually used to calculate the amount of emission electrons. In this model, the net injected current is calculated by subtracting the emission current from the probe

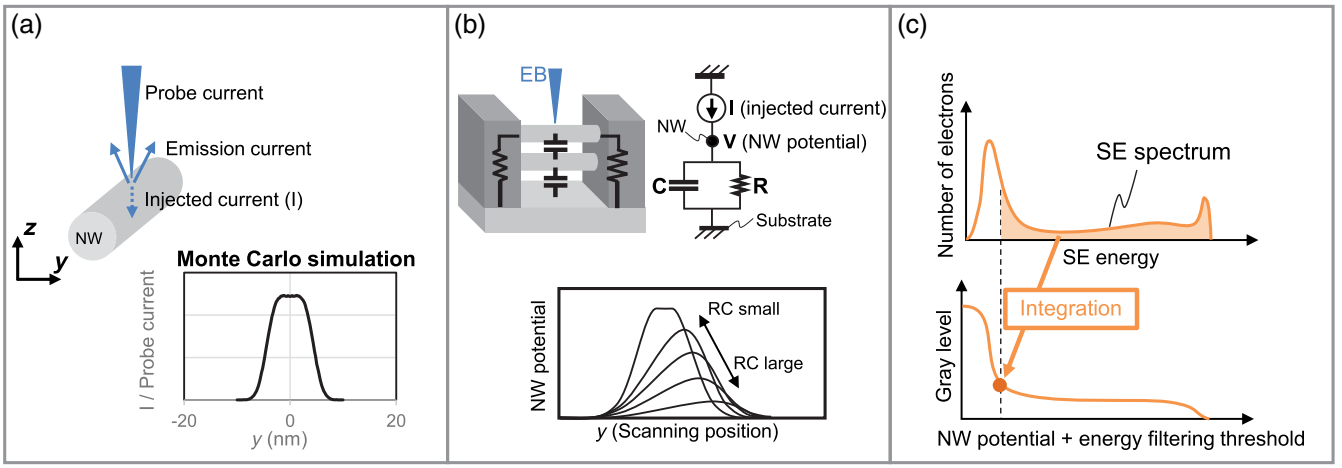

Fig. 5 Overview of the proposed model to calculate VC. (a) Injected current calculation step, (b) NW potential calculation step, and (c) gray-level estimation step.

current. The plot in Fig. 5(a) shows an example of the injected current as a function of position, y, when EB is scanning across a 10-nm-diameter NW. It should be noted that the injected current—namely SE emission—is larger at the NW center, which is different from a usual case that SE profile has peaks at sample edges. This is because the NW is smaller than the scattering region of primary electrons. The SE peaks at edges had merged into single peak at the center. Subsequently, the position-dependent injected current, $I(y)$, is converted into time-dependent current, $I(t)$, considering the scan speed.

The second step [Fig. 5(b)] is to calculate the time-dependent NW potential, $V(t)$, from time-dependent injected current, $I(t)$. The model considers an equivalent circuit, which consists of resistance, R, and capacitance, C. They are a combination of all resistance and capacitance existing between the top NW and the substrate, for example, top-NW to bottom-NW capacitance and bottom-NW to substrate capacitance, as shown in Fig. 5(b). With this circuit, time-dependent NW potential, $V(t)$, can be calculated from $I(t)$ by the following equation:

$$\frac{\mathrm{d}V(t)}{\mathrm{d}t} = \frac{I(t)R - V(t)}{RC}. \tag{1}$$

Subsequently, the time-dependent NW potential, $V(t)$, is converted back into position-dependent NW potential by considering the scan speed again. The lower plot schematically shows the NW voltage evolution expected from Eq. (1). This plot does not mean that the NW potential has a special distribution but expresses the NW potential as of the time when EB is scanning at that position. When RC is small, the NW potential should rapidly become equilibrium as follows:

$$V(t) = I(t)R. \tag{2}$$

With increasing RC, the NW potential change should be delayed. Thus, the timing of the potential peak is shifted later. Such charging dynamics can be formulated with this model.

The third step [Fig. 5(c)] is to estimate the gray level of SEM images. The amount of the detected electrons from the top NW can be estimated by integrating the SE spectrum above the cutoff energy, which is the sum of NW potential and threshold of energy filtering. Thus, the relationship between the NW potential and the gray level can be obtained by measuring or assuming the SE spectrum. The position-dependent gray level (hereafter called "VC profile") can be estimated from the position-dependent NW potential, which is obtained in the second step.

It should be noted that the amount of the detected electrons (gray level) is determined by the emission current and the surface potential. For example, the emission current is large at the NW center [Fig. 5(a)]. However, it means that injected current is also large so that the surface potential would be high—to mention exactly, it depends on the time-dependent potential evolution—and the fraction of SEs passing the filter should be decreased. Consequently, gray level decreases. Such a trade-off can be formulated with the model.

3 Results and Discussion

3.1 *Nanowire–Source/Drain Contact Inspection Result by Voltage Contrast*

Figure 6 shows typical SEM images acquired with and without energy filtering of SEs. One of the NWs clearly appeared

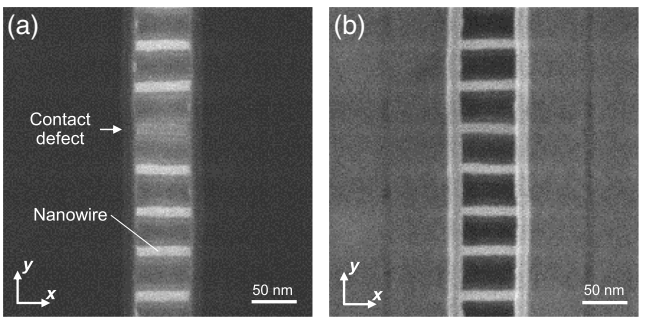

Fig. 6 Typical SEM images of 70-nm-long NWs. (a) An SEM image acquired with energy filtering of SEs. (b) A SEM image acquired without energy filtering. Both images were taken with 800-V accelerating voltage, 8-pA probe current, and middle-speed scan along x axis. They are the same NWs. VC is clearly observed by energy filtering.

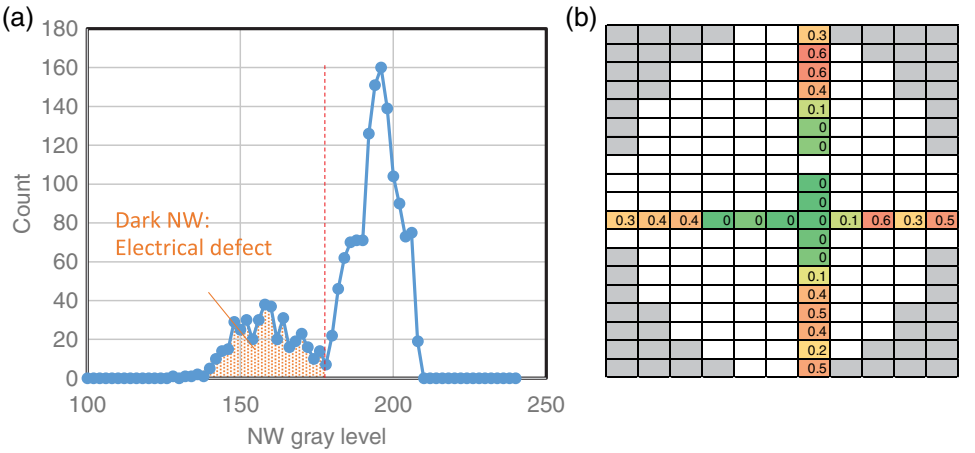

Fig. 7 (a) Gray-level histogram of 1680 70-nm-long NWs. Gray level was extracted from the VC images taken with 800-V accelerating voltage, 8-pA probe current, and middle-speed scan along *x* axis (parallel to NWs). The dashed line is a criterion between dark NWs and bright NWs. The dark NWs should correspond to the electrical defects. (b) Intrawafer map of the ratio of defect NWs. Electrical defects are more frequent at wafer edge.

darker than other NWs in the image with energy filtering (hereafter called "VC image") [Fig. 6(a)], though the gray level of all NWs is almost the same without energy filtering [Fig. 6(b)]. It means that gray level decrease is VC, which is caused by the charging of the top NW, namely, there is an electrical contact issue in the dark NW. This result suggests that VC is effective for the contact inspection of NW FETs.

Figure 7(a) shows the histogram of mean gray level of 1680 NWs observed with energy filtering. It was confirmed that all NWs are existing at the proper position by the SEM observations without energy filtering. Clearly, the histogram has two peaks. They should correspond to the NWs with electrical defect (darker NWs) and normal NWs (bright NWs). A dashed line in Fig. 7(a) should be a good criterion to separate the defect NWs and the normal NWs. The fraction of defective NWs in each inspected die is shown as a wafer map in Fig. 7(b). This inspection revealed that the electrical defects are more frequent at wafer edge than at wafer center. Such data should be valuable for process monitoring and failure analysis of the contact issue.

3.2 *Verification of Inspection Result with TEM*

The obtained cross-sectional TEM images are shown in Fig. 8, together with the VC images of the same NWs. The epitaxial growth of SD is not sufficient to reach to the top NWs level in general. In some cases, the top NW is connected to SD through a narrow oblique bridge (indicated by white arrows in Fig. 8). In other cases, the NW is not connected to SD region. All bottom NWs are well connected to SD. Comparison between the TEM images and the VC images clarifies that the dark NWs in VC images are floating NWs, which have contact defects at both ends. If NW is connected to SD at least at one side, it appeared bright in a VC image. Such correspondence is confirmed in all tested NWs. This result verifies the validity of the VC-based inspection of NW–SD contact, although the inspection is limited to the floating NW detection and not effective to detect the one-side defect.

3.3 *Resistance and Capacitance Estimation*

Figure 9 shows the VC images taken at the same field of view with different scan speeds and directions. VC was clearly observed regardless of the scan speed in case of scanning along *x* axis (parallel to NWs). In contrast, VC was less significant for faster speed scan in case of scanning along *y* axis (across NWs). This tendency can be interpreted by considering the duration of continuous EB irradiation on single NW, which is 0.19, 1.5, and 12 μs, for high-, middle-, low-speed scans, respectively. The NW potential due to EB-induced charging should be lower for faster scan because the continuous EB irradiation duration is the shorter for the faster scan.

For a detailed analysis, VC profiles of the NW were extracted from Figs. 9(d)–9(f), as shown in Fig. 10. They were taken from the same NW with different scan speeds. Figures 10(a)–10(d) show no decrease of gray level. It means no charging happened on the NWs A-D. On the other hand, Figs. 10(e)–10(g) show a clear SEM signal suppression, namely, VC. One remarkable feature in Figs. 10(e)–10(g) is that VC is particular at around the NW center. This is because the higher injected current at NW center [Fig. 5(a)] caused the higher NW potential, which resulted in the larger VC although the total emission current was higher at NW center. Another remarkable feature is that the suppressed profiles are asymmetric. This is due to the charging dynamics, as describe in Fig. 5(b). In other words, the NW potential increases during the scan on the NW if relaxation time is longer than the scan duration. The NW potential is higher when the EB scanning at the latter half of the NW (right side in Fig. 10). The SEM signal suppression due to VC is, therefore, more evident at right side. These features imply that a quantitative evaluation of these VC profiles would enable the estimation of parasitic resistance and capacitance.

Parasitic resistance and capacitance were estimated by finding the best-fit parameters in the proposed VC model to reproduce the experimentally obtained VC profiles. Figure 11 shows the results of systematic model calculation. About 16 combinations of resistance, *R* (100, 200, 400, and

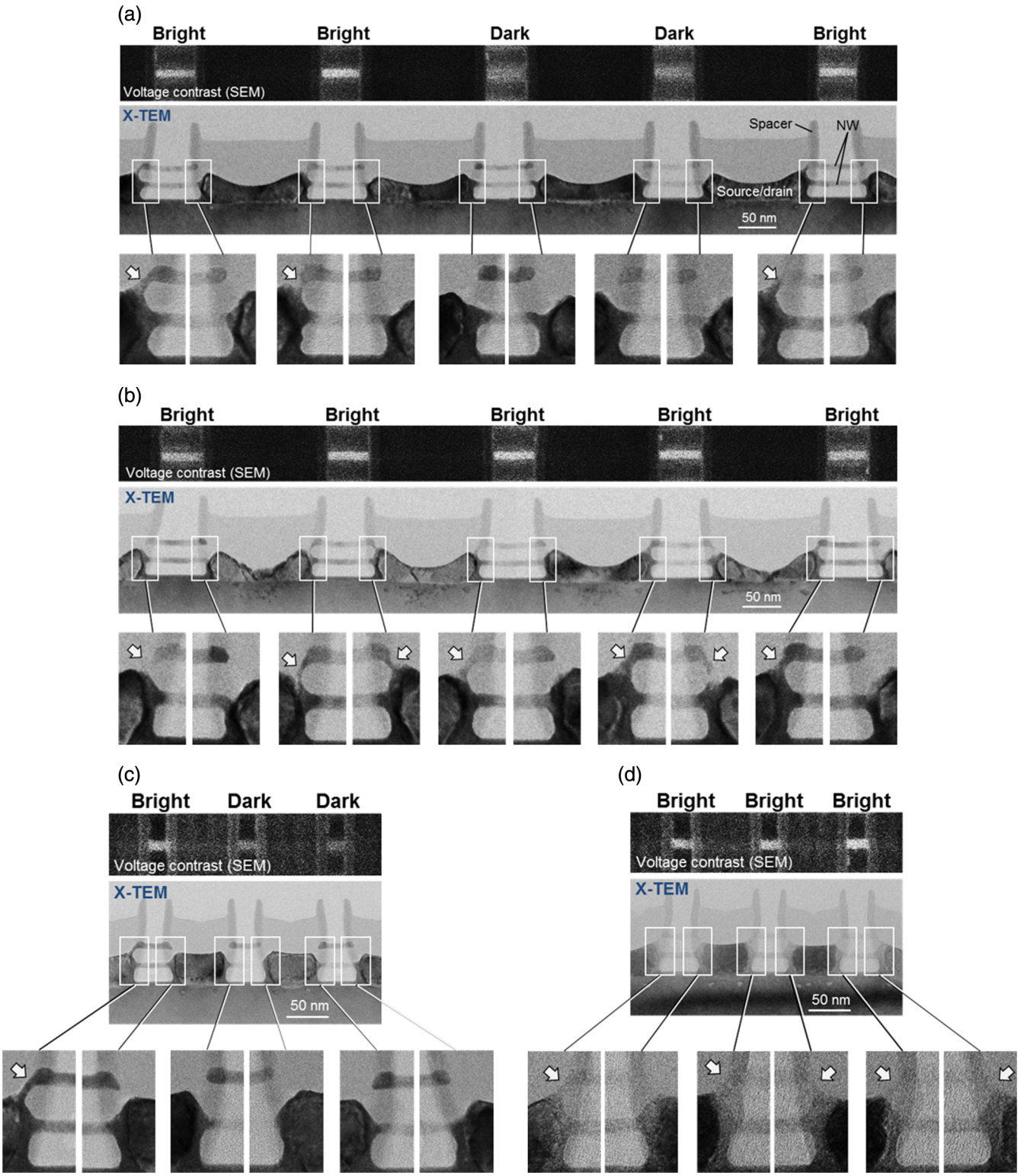

Fig. 8 Comparison between SEM VC images and cross-sectional TEM images of the NWs. (a) 70-nm-long NWs at wafer edge, (b) 70-nm-long NWs at wafer center, (c) 28-nm-long NWs at wafer edge, and (d) 28-nm-long NWs at wafer center. White arrows in enlarged TEM images are indicating that NW and SD are connected through a narrow bridge.

800 GΩ) and capacitance, C (1, 2, 4, and 8 aF) were used as input parameters of the model calculation. Other model conditions, such as accelerating voltage, probe current, and scan speed, were set the same as the experimental conditions. The characteristic features discussed in the previous paragraph, namely, the signal decrease at the center and the asymmetric profile, were reproduced by the model calculation. It suggests that the proposed model adequately describes the

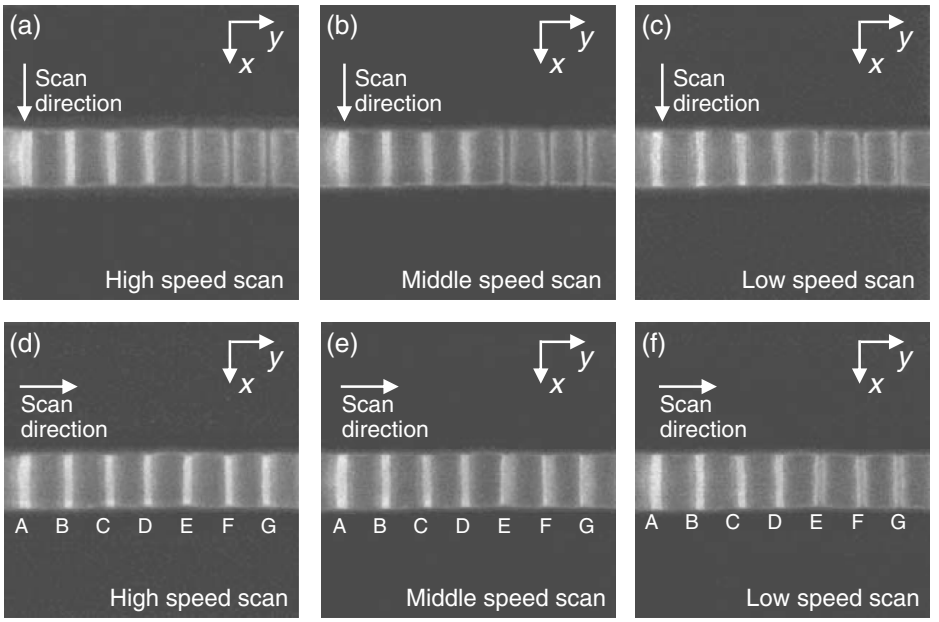

Fig. 9 VC images with different scan speeds and directions. (a)–(c) Scan parallel to NWs with high-, middle-, and low-speed scans, respectively. (d)–(f) Scan across NWs with high-, middle-, and low-speed scans, respectively. Capital letters A to G indicate NWs whose profiles are shown in Fig. 10.

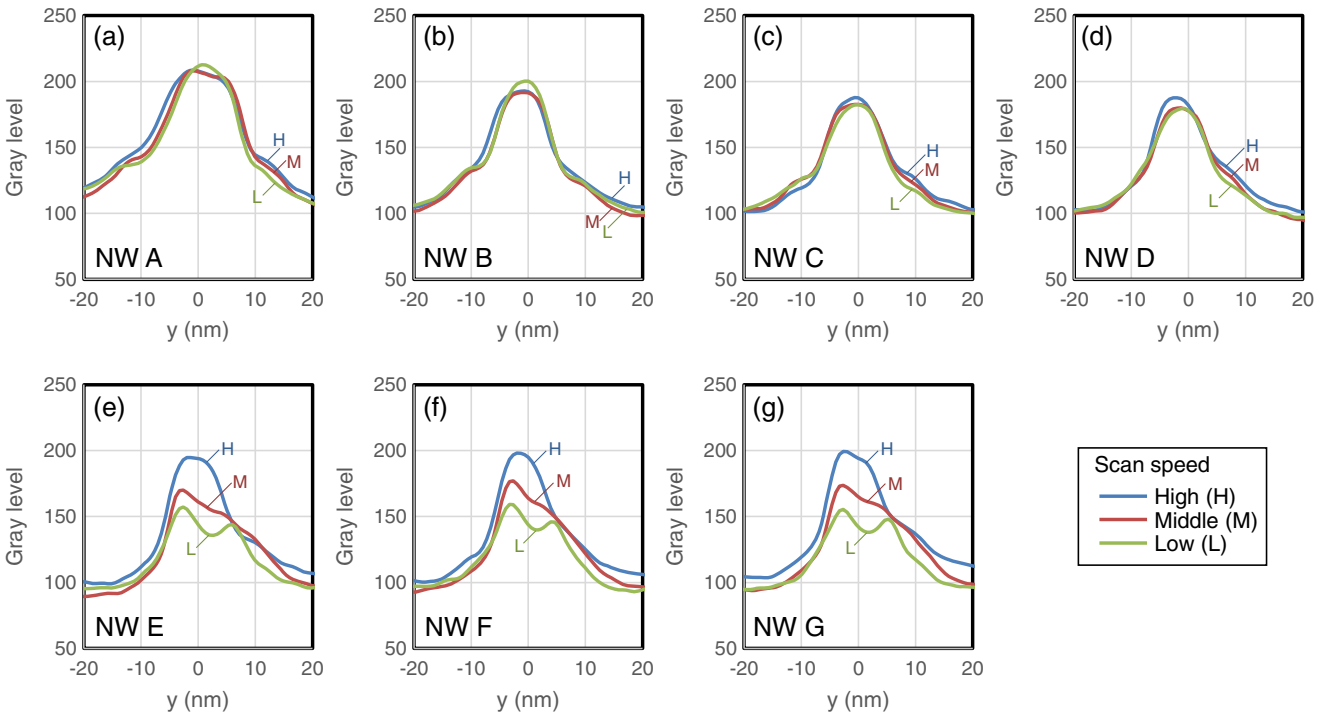

Fig. 10 VC profiles of the NWs: (a)–(g) correspond the NWs A to G in Figs. 9(d)–9(f).

charging dynamics. Among the calculated series of profiles, the result with $R = 200$ GΩ and $C = 2$ aF matches the experimental results (Fig. 10) most similarly. This matching should be reliable because it is based not only on the shape similarity of each profile but also on the trend similarity of scan-speed dependence. Therefore, the resistance and capacitance were estimated to be 200 GΩ and 2 aF, respectively. Such quantitative evaluation should be valuable for more accurate inspection.

In addition, the capacitance measurement gives the information on the defect point where the electrical connection is hindered. The capacitance between the top NW and the bottom NW can be calculated by the following analytical equation:

$$C = \frac{l\pi\varepsilon_0}{\log\left[\frac{h}{a} + \sqrt{\left(\frac{h}{a}\right)^2 - 1}\right]}, \tag{3}$$

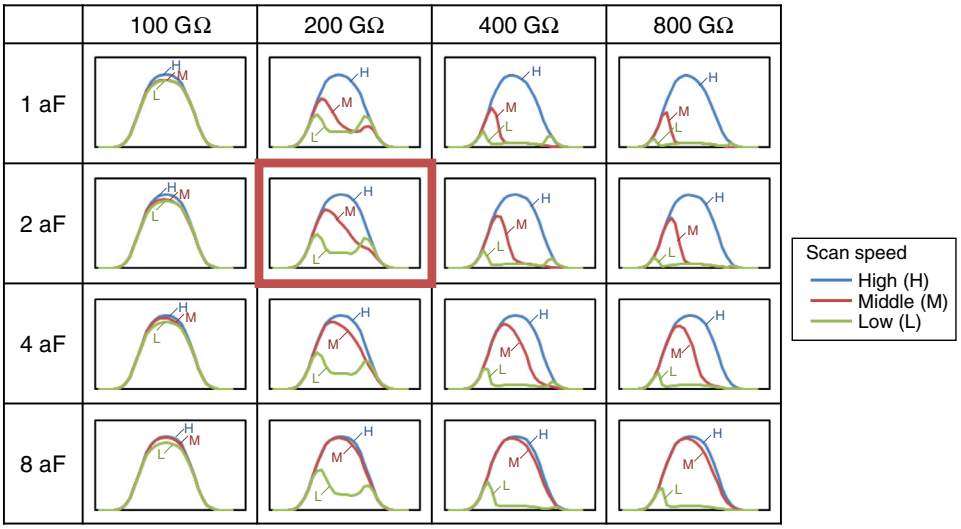

Fig. 11 VC profiles calculated by the proposed VC model. About 16 combinations of resistance ($R = 100$, 200, 400, and 800 GΩ) and capacitance ($C = 1$, 2, 4, and 8 aF) were used as input parameters of the model. Among these series of VC profiles, the result with $R = 200$ GΩ and $C = 2$ aF is most similar to the experimental result.

where a is the wire diameter, h is the distance between two stacked NWs' center, and l is the NW length. By approximating $a = 10$ nm, $h = 20$ nm, and $l = 70$ nm according to the actual NW dimension, the capacitance between stacked NWs is found to be about 3 aF. The value is consistent with the measured capacitance. It suggests that top NW is electrically disconnected from the lower one. Thus, most probable defect point is the interface between the top NW and SD. Such a presumption is possible by measuring the parasitic capacitance without performing the physical analysis, such as cross-sectional TEM.

4 Summary

A methodology to evaluate the electrical contact between NW and SD in NW FETs was investigated. The NWs with electrical defect were clearly detected by the SEM signal decrease in VC images acquired with energy filtering of SEs. Comparison with cross-sectional TEM observations verified the correspondence between the VC and the NW–SD contact condition. This result confirms that a robust NW–SD contact inspection of NW FET is possible by means of VC, although the inspection is limited to the NW with defects on both ends.

Moreover, estimation of the parasitic resistance and capacitance was achieved. We proposed a VC model that considers the dynamics of EB-induce charging based on *RC* equivalent circuit. The model can calculate the SEM profiles by assuming resistance and capacitance as floating parameters. Meanwhile, the experimental SEM profiles strongly depended on the EB scan speed due to the charging dynamics. Thus, the resistance and capacitance can be determined by finding the best parameters to reproduce the experimental profiles. In our feasibility test, the parasitic resistance and capacitance of 70-nm-long NW with electrical defect were estimated to be 200 GΩ and 2 aF, respectively. The estimated capacitance is roughly consistent with the capacitance between the vertically stacked two NWs. It suggests that the top NW is electrically disconnected from the bottom NW and that there is a contact issue between the top NW and SD region. Quantitative estimation of resistance and capacitance would be valuable not only for accurate contact inspection but also for identification of the defect point.

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