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Ho Ju Kang
Sang Uk Cho
Eung Soo Kim
Chang-Seok Kim
Myung Yung Jeong

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Ho Ju Kang

Sang Uk Cho

Pusan National University
Department of Cogno-Mechatronics Engineering
Geumjeong-gu, Busan, Republic of Korea

Eung Soo Kim

Pusan University of Foreign Studies
Departments of Digital-Media
Nam-gu, Busan, Republic of Korea

Chang-Seok Kim

Myung Yung Jeong

Pusan National University
Department of Cogno-Mechatronics Engineering
Geumjeong-gu, Busan, Republic of Korea
E-mail: myjeong@pusan.ac.kr

Abstract. Here, we present a new double-side patterned sapphire substrate methodology that improves the efficiency of gallium nitride-light emitting diodes (GaN-LEDs). The light extraction efficiency of GaN-based LEDs was analyzed through the use of a ray-tracing simulation. The extraction efficiency was simulated using patterned sapphire substrate LEDs with a variety of shapes, depths, sizes, and spacing. Through the optimal patterning of the various factors, high extraction efficiency was realized and subsequently improved upon. The thermal LED characteristics were analyzed through the use of the COMSOL general heat transfer module. The LEDs patterned on the sapphire substrate were fabricated using nano imprint lithography. We found that the output power of the double-side patterned LED was 52% greater than that of a flat LED. The thermal resistance of the double side patterned LED was 9.5 K/W less than that found for the flat LED. © The Authors. Published by SPIE under a Creative Commons Attribution 3.0 Unported License. Distribution or reproduction of this work in whole or in part requires full attribution of the original publication, including its DOI. [DOI: [10.1117/1.OE.52.2.023002](https://doi.org/10.1117/1.OE.52.2.023002)]

Subject terms: light emitting diode; patterned sapphire substrate; nanoimprint lithography; double side patterned sapphire substrate.

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1 Introduction

As the lighting industry continues to advance, the light emitting diode (LED) market share is increasing explosively. The biggest reason for this growth is that LEDs are more energy efficient and have a longer life compared with conventional light sources. The era of full-scale LED applications has arrived as blue and white gallium nitride (GaN) semiconductor based LEDs are commercialized. The LEDs offer the benefits of fast processing speed of a semiconductor and low electricity consumption. As such, they have been accepted into the strategic national product for green growth. The development of the blue GaN LED in the mid-1990s enabled the full-color LED displays that have become a common feature in our daily lives. The high intensity LED market is expanding too fast to measure; efforts to enlarge the chips, improve their luminous efficiency, and the enhancement of their heat dissipation technology support are actively ongoing. However, LEDs have their own problems. The biggest problem is that LED prices are 20 times more expensive than conventional lighting; this is a big burden for their use in households and offices. In order to develop low cost, high intensity LEDs for lighting, more studies regarding luminous efficiency improvement and heat dissipation system development are needed.^{1,2}

There have been many studies regarding increased LED efficiency. The patterned sapphire substrate (PSS) method has been reported to not only improve light extraction efficiency but also increase the internal light efficiency through a low dislocation effect when growing an epitaxial layer growth on the top of the sapphire substrate.³⁻⁶ However, these studies are mostly based on lab experiments that are used to show if the efficiency is increased compared to the existing LEDs, which means the quantitative results

are somewhat lacking. In order to quantitatively analyze the efficiency improvement from a PSS design, an LED has to pass through many processes. However, there have been studies that quantitatively analyze the improvement of light extraction efficiency through a PSS design in order to develop low cost high intensity LEDs.^{1,2,7}

This study proposes a new structure that utilizes double-sided patterns on the sapphire substrate in order to increase the light extraction efficiency and heat dissipation efficiency. A Light Tools 7.0 simulation program applying Monte Carlo Method based ray tracing was used to quantitatively analyze the light extraction efficiency of the PSS and to design the pattern. A COMSOL heat transfer simulation was used to analyze the improvement in the heat dissipation efficiency. The designed pattern was applied using a nano imprint lithography (NIL) method to create the pattern on the sapphire substrate used to fabricate and evaluate the actual LED sample.

2 Simulations

For this study, a planar figure of a typical LED chip structure was modeled, as shown in Fig. 1. The modeled GaN based LED chips shown in Fig. 1 have an area of $350 \times 350 \mu\text{m}^2$ and a thickness of $85 \mu\text{m}$. The thickness of the sapphire substrate in the multilayered structure is $80 \mu\text{m}$. An n-GaN layer with a $4 \mu\text{m}$ thickness was placed on the sapphire substrate and a multiquantum well (MQW) with a 100 nm thickness was placed on top of it as the active layer. A $1\text{-}\mu\text{m}$ -thick p-GaN layer was then added. A 300-nm -thick transparent electrode indium tin oxide (ITO) layer was added to the top layer. Since the bottom of the LED element is the printed circuit board and thus does not pass any light, the bottom part of the LED was modeled to be reflective. Table 1 shows the optical

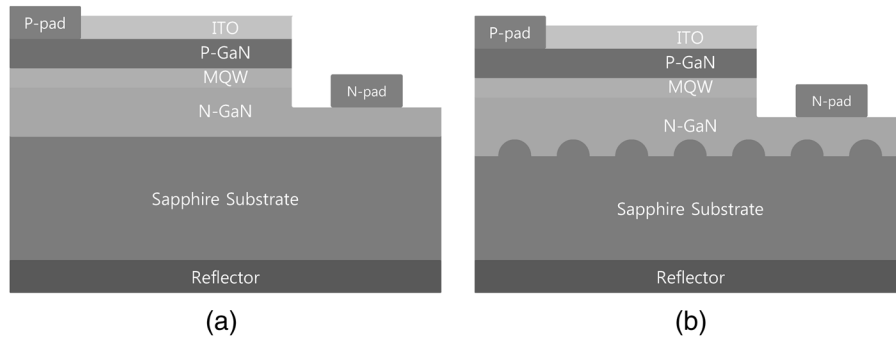


Fig. 1 The modeling of the LED structures: (a) the nonpatterned LED structure and (b) the patterned LED structure.

Table 1 The optical properties of the LED etch layers.

Layer	Refractive index	Optical absorption (/mm)
Sapphire	1.71	0
GaN	2.39	8
n-GaN	2.61	8
MQW	2.61	8
p-GaN	2.43	8
ITO	1.9	0
Epoxy	1.41	0

properties of the LED components. For the refractive index, the sapphire is set to 1.71, the air to 1, the p-GaN layer to 2.43, and the n-GaN layer to 2.61. In the case of the MQW, the refractive index of the multiple layers was set to 2.61. Epoxy with a refractive index of 1.41 was used for the LED chip encapsulant. When light is emitted from the LED element, the critical angle is around 23 deg, since the element and air have a refractive index of 1. This means that only the light within the critical angle of 23 deg can be emitted outside. An accurate simulation epoxy was used for the LED element encapsulant.

Another optical property that must be considered is the absorption. The absorption factor depends on the medium. Table 1 shows the absorption coefficients of the different media applied in this study.^{3,8}

To run the simulation, the light source and receiver must be set up after the structure is designed. As the light source, the active MQW layer is set up as the cubic light source. A total of 100 million sample light rays are emitted randomly in all directions from an arbitrary position in the MQW layer. The receiver measured the far field radiation power in order to detect the rays and measure the light extraction efficiency of the LEDs.

In order to observe the change of the light extraction efficiency according to the shape of the pattern created on top of the sapphire substrate, patterns for seven different shapes: hemispheric, conical, truncated-cone, pyramidal, truncated-pyramid, square pillar, and cylindrical were designed (Fig. 2). Each shape was designed considering the bumps and holes in regards to the etching of the sapphire substrate.

The height, depth, diameter, and spacing between the patterns were changed for each pattern shape in order to observe the changes in the light extraction efficiency (Fig. 3). To obtain large changes in value, hole-shaped patterns were used for the simulations. Bump-shape patterns were excluded since they cannot be higher than the GaN layer formed on top of the sapphire substrate. Figure 4 presents the changes in the light extraction efficiency according to the shape of the pattern on the sapphire substrate layer. The bump and hole shapes for the hemisphere, cone, truncated-cone, pyramid, truncated-pyramid, square pillar, and cylinder patterns shown in Fig. 2 were compared. The PSS pattern used in the simulation had a diameter of

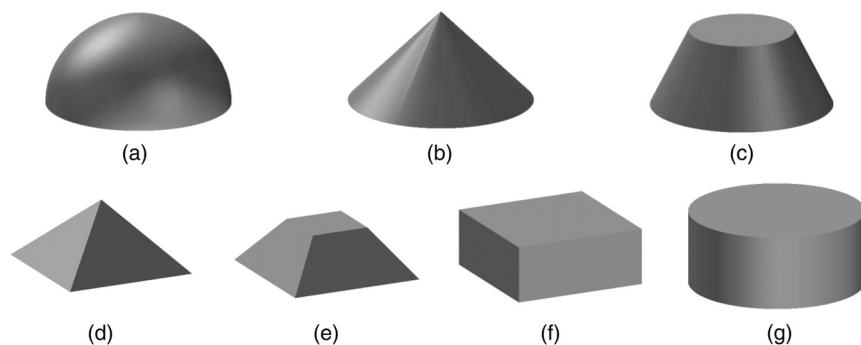


Fig. 2 The modeling of the patterns on the sapphire substrate. (a) Hemisphere, (b) cone, (c) truncated-cone, (d) pyramid, (e) truncated-pyramid, (f) square pillar, and (g) cylinder.

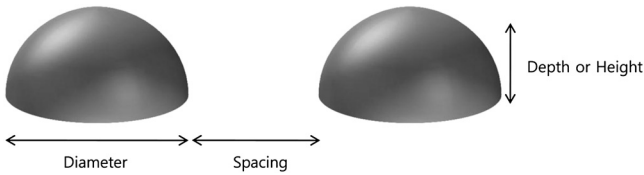


Fig. 3 The hemispherical patterns and their specific sizes.

3 μm , pitch of 6 μm , and a height of 3 μm . Figure 4 shows the light extraction efficiencies comparison according to the pattern shape on the sapphire substrate. As shown in Fig. 4, the cone-shaped bump had the largest light extraction efficiency at around 36.5%. The hemisphere also had a high light extraction efficiency of around 35.4%. The first insight would indicate that the hemisphere would have the highest efficiency because all of the incidental light would be perpendicular to the surface. However, since the numerous light rays that are emitted in a three-dimensional structure are determined by the minimization of the reflection that reduces the probability of it passing through the absorption layer resulting in the probability of the reflection angle

changed by the pattern stays within the critical angle between the GaN and the epoxy. Therefore, there are differences according to the pattern shape, which is why the cone structure had the highest light extraction efficiency. The differences between the bumps and holes were relatively higher in the cone pattern and cylinder patterns. This is probably because of the difference of the bump and hole shapes, as the number of light rays crashing to the sidewall was smaller for the hole shape. Since the diameter of the pattern plays the role of the aperture that lets the light pass through the hole shape, the circular structure hole shape had the lowest efficiency because its area was the smallest for the same diameter.

When the hole depth increased to around 2 μm , the light extraction efficiency increased. On the other hand, when the depth increased by more than 2 μm , the efficiency decreased. In a certain pattern diameter, an increase in the pattern depth reduces the total internal reflection of the light ray, increases the transmission, and diffuses the reflection of the incident light; however, it is affected by the diameter and depth. The efficiency increases when the angle of the light that penetrates inside the pattern and is reflected from the side wall

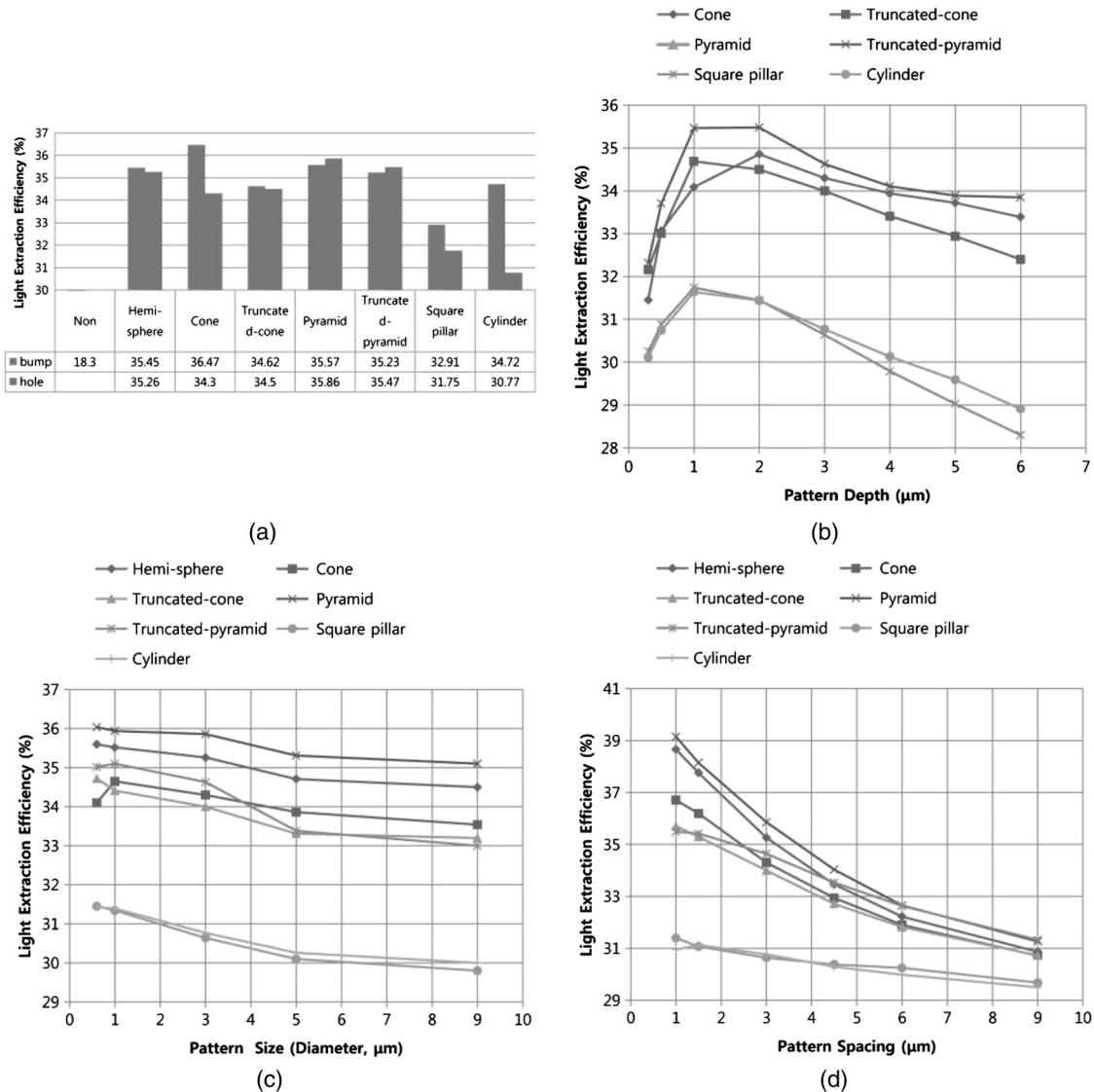


Fig. 4 The extraction efficiency according to the patterns: (a) shape, (b) depth, (c) size, and (d) spacing.

at an angle larger than the critical angle; however, the light is absorbed again when the depth exceeds a certain value. The test indicates that the efficiency is high when the aspect ratio of the depth and diameter is around 3:1 or 3:2. As the pattern size decreased, the light extraction efficiency increased. This is because the light extraction efficiency increased as the number of patterns per unit area increased. However, when the number of patterns is high or the diameter is large, the dislocation of the thin film makes this unfeasible. Considering the thin film growth condition, the pattern size was selected to be within 5 μm. It is important to find the process conditions needed to increase the number of patterns in a unit area. As the pitch decreases, the number of patterns increase and the light extraction efficiency greatly increases. This results in an increase in the diffuse reflection probability by patterns per unit area. This also means that the impact to the light extraction efficiency is great when the space between the patterns is in nanometer size. The study shows that the light extraction efficiency increased to around 39% when the pattern pitch was 1 μm. As such, the highest light extraction efficiency is expected when the patterns are uniform and there are a high number of patterns, i.e., the nano patterning structure. We optimized the pattern design for high efficiency LED considering the simulation result. When the pattern has 600 nm diameter and 300 nm height, the extraction efficiency increased around 45%.

The heat created by the LED chip is mostly transmitted to the package through conduction by the paste and heat slug directly in contact with the chip. This study observes the changes in the temperature according to the pattern. Equation (1) was used as the governing equation for the simulation. It is the heat equation resulting from conduction and convection and excludes the impact of radiation.

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k \nabla T) = Q - \rho C_p \nabla T, \quad (1)$$

where ρ is the material density, C_p is the specific heat, k is the thermal conductivity, and Q is the heat source. Since

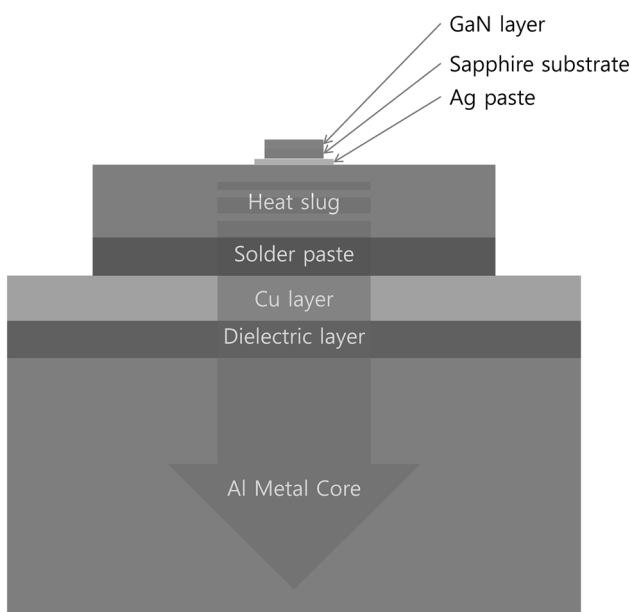


Fig. 5 The modeling of the LED structures for the heat transfer simulation.

Table 2 The thermal properties of the LED each layers.

Materials	Thermal conductivity (W/m * K)	Thickness (μm)
GaN	65.6	5
Sapphire	30	80
Ag paste	20	25
Heat slug	385	1,000
Solder paste	5	50
Dielectric layer	1.5	50
Al Metal Core	180	1,500

natural convection is the typical cooling method for LEDs, the heat transfer coefficient of 10 W/m² · K was applied for the natural convection between the LED element surface and the atmosphere. Figure 5 is modeling of LED for heat transfer simulation. Table 2 is thermal properties of the LED layers. Figure 6(a) shows the thermal characteristic of a typical LED element without the pattern increases up to 130.34°C. Figure 6(b) shows the thermal characteristic of the LED element with the pattern at the bottom of the sapphire substrate at 128.58°C. This indicates that there is a temperature difference of 1.7°C according to the existence of the pattern. Considering that it is a small LED element with a dimension of 300 × 300 μm², the improvement in the heat dissipation characteristic is expected to be greatly enlarged if the pattern area is increased.

3 Nanoimprint Lithography

The NIL method using thermal and ultraviolet (UV) resist was used to transfer the pattern designed with the patterning process to the sapphire substrate.⁹⁻¹¹ Fabrication process flow is shown in Fig 7. First, the patterning of the sapphire substrate was carried out by NIL process using Si mold. The sapphire substrate was then dry etched using inductively coupled plasma (ICP) etching machine. And finally, we fabricated double side patterned sapphire substrate by NIL, etching process on single sapphire substrate. Since the thermal resist has a suitable adhesive strength, it is securely glued to the substrate during the de-molding process. In the NIL process, spin coating sprayed the resist at the velocity of 3000 to 6000 rpm. For the NIL process, the temperature was set to 180°C for 8 min for hardening and the UV was irradiated for 60 s. The pressure was set at 3 to 20 bars and the demolding temperature was cooled down to 70°C before the stamp was removed. Figure 8 shows scanning electron microscope image of the 585 nm pattern after the NIL process is completed. In order to fabricate the patterned sapphire substrate, a dry etching process was executed using ICP equipment. The ICP power was set at 700 W and the radio frequency (RF) was applied at 200 W for 600 s. BCl₃ and Cl₂ were used as the gas, and a 2 mTorr pressure was applied.

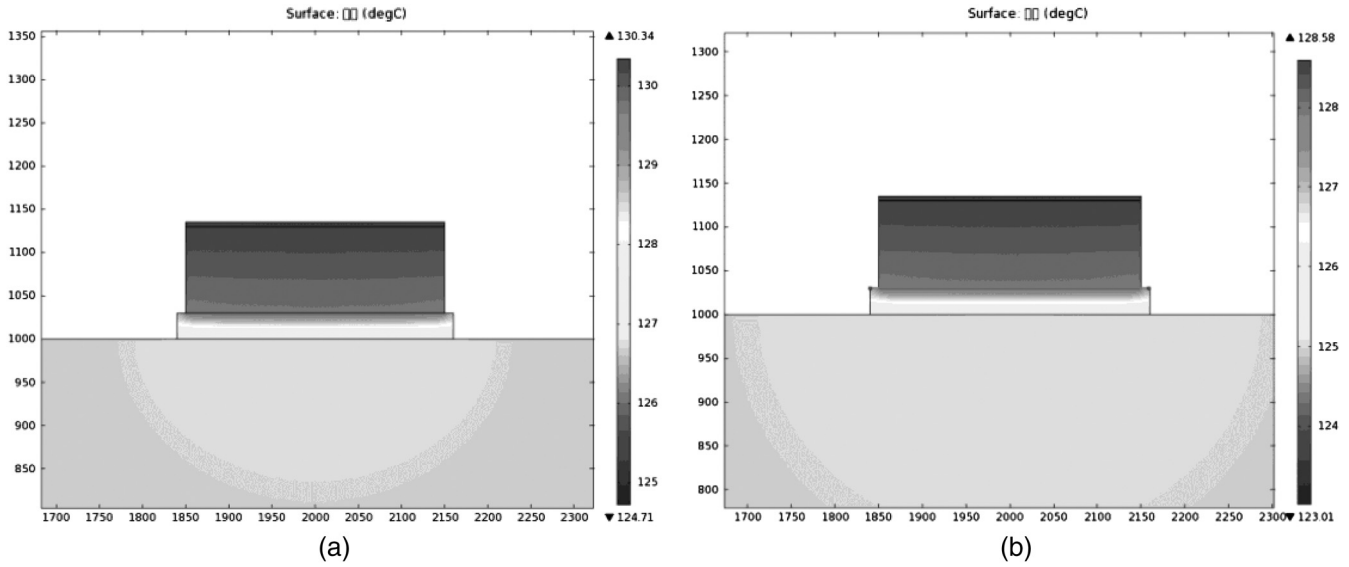


Fig. 6 Thermal degree according to LED chip (a) normal sapphire substrate and (b) patterned sapphire substrate.

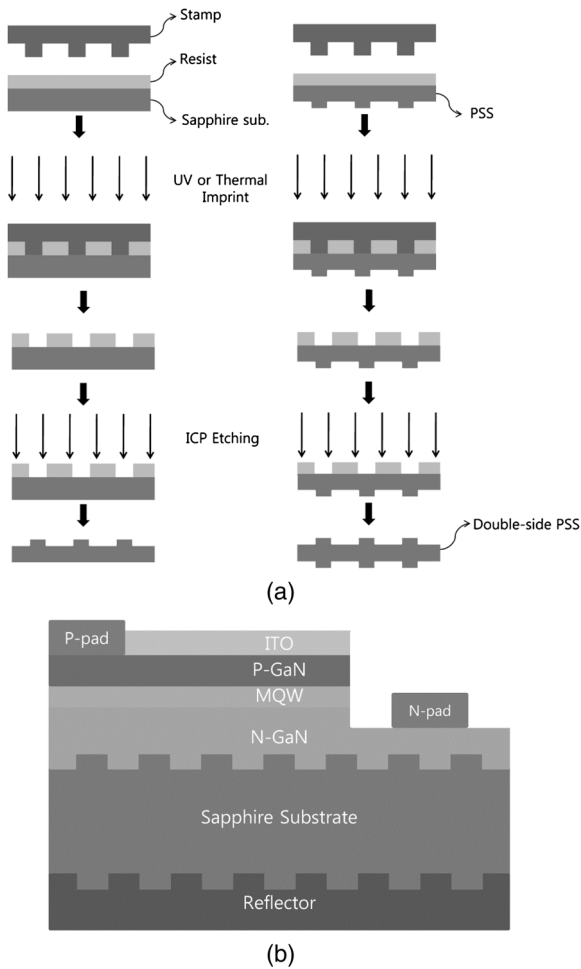


Fig. 7 Schematic diagram of double side patterned sapphire substrate fabricating method.

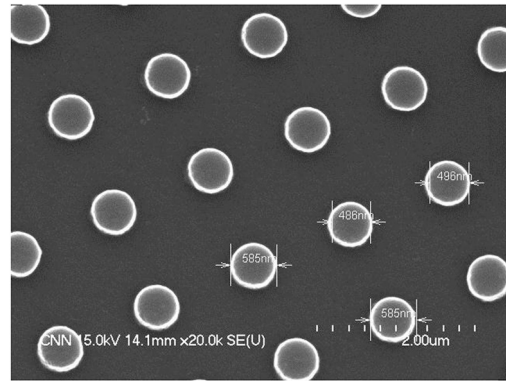


Fig. 8 The SEM image of the patterned sapphire substrate after NIL process.

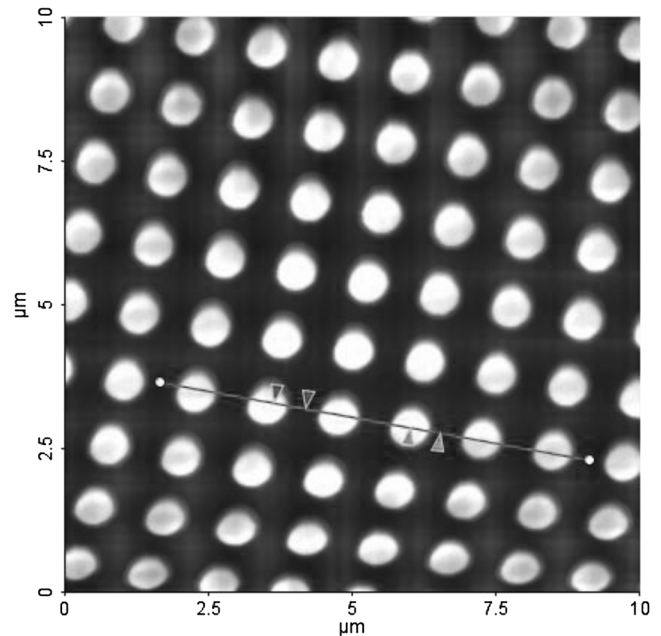


Fig. 9 The AFM results of the etched sapphire substrate.

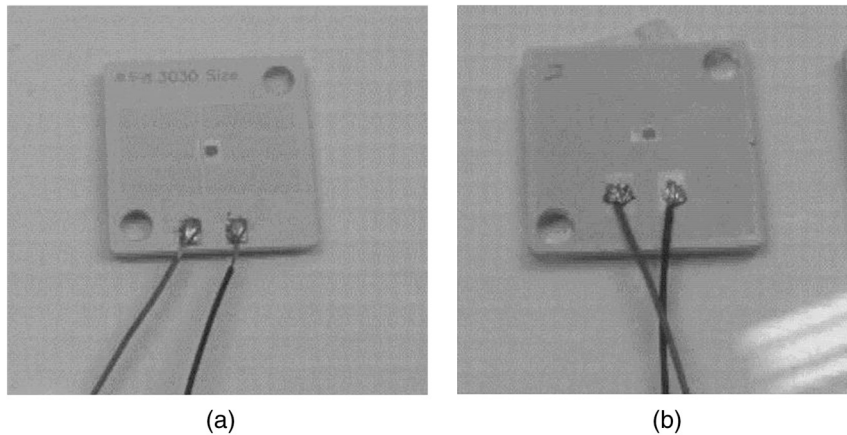


Fig. 10 Image of LED sample used (a) normal sapphire substrate and (b) double side patterned sapphire substrate.

Table 3 The I/V characteristics, radiation flux and thermal resistance for the LED samples.

	Input voltage (V)	Input current (mA)	Radiation flux (mW)	Thermal resistance (W/K)
Normal	3.441	350.0	308.2	32.49
PSS	3.311	350.0	469.5	22.54

- Process pressure: 2 mTorr
- Gas flow rate: BCl₃/Cl₂ (50 scum)
- RF power: 200 W
- ICP power: 700 W

Figure 9 shows the values measured using an atomic force microscope after the etching process using ICP. Patterns with a 290 nm height and 580 nm diameter were created. The MOCVD process and packaging process were then executed in order to fabricate the LED element samples. Figure 10(a) is LED sample using normal sapphire substrate and Fig. 10(b) shows LED sample using double side patterned sapphire substrate. Afterward, properties such as the radiant flux and thermal resistance of the LED samples were measured (Table 3).

4 Conclusion

Double-side patterns were formed on a sapphire substrate in order to create high efficiency LEDs. In this study, we simulated PSS-LED devices using a ray tracing method based on the Monte Carlo Method. The extraction efficiency was simulated using the patterned shape, size, depth, and period. The role of the patterned sapphire substrate in PSS-LED was analyzed and discussed; the thermal characteristics of the LEDs were analyzed using the Comsol general heat transfer module.

NIL is a technology that can easily print dozens of micro and nano patterns. The LEDs patterned on the sapphire substrate were fabricated using NIL to improve efficiency. NIL was used to make nano-scale bump patterns on a double-side sapphire substrate. The samples were grown on sapphire substrates through metal organic chemical vapor deposition. The output power of the double side

patterned LED was 52% higher than that found for the flat LED, and the thermal resistance of the double side patterned LED was 9.5 K/W smaller than that found for the flat LED.

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Ho Ju Kang received his MS degree from Pusan University, Busan, Republic of Korea, in 2012. He is currently working toward the PhD degree at Pusan National University, Busan, Republic of Korea. His research interests include LED, OLED, and lithography.



Sang Uk Cho is currently working toward the PhD degree at Pusan National University, Busan, Republic of Korea. His research interests include roll-to-roll lithography, nano imprint lithography, and optical devices.

of Korea Telecom, Daejeon. His work was supported by the Korean Government Overseas Study Scholarship. In 2004 and 2005, he was a postdoctoral researcher with Beckman Laser Institute and Medical Clinic, University of California, Irvine. He joined Pusan National University, Busan, in 2005 as an assistant professor. Since 2009, he has been an associate professor in the Department of Cogno-Mechatronics Engineering, Pusan National University. His research interests include development of novel fiber laser systems and their application into biomedical, telecommunication, and sensor areas.



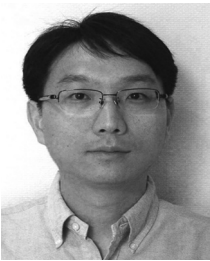
Eung Soo Kim received his BS and MS degrees in electronics engineering from Kyungpook National University, Korea in 1990 and 1992, respectively. He received the PhD degree in material science from Faculty of Science and Technology, Keio University in Japan in 1996. He has been a visiting professor in Department of Electronics Engineering at Keio University in Japan. He received a JSPS Fellowship in 2003. He has been the head of the

Institute of Information & Communication in Pusan University of Foreign Studies from 2008 to 2010. He is currently a professor in division of digital media engineering, Pusan University of foreign studies. His research interests include optical sensor, nonlinear optics, optical waveguide devices, polymer optical fiber, and optical integrated circuits.



Myung Yung Jeong received BS and MS degrees from Pusan National University, Pusan, Korea, in 1982 and 1984, respectively, and the PhD degree from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2000. Since September 1983, he has worked for the Electronics and Telecommunications Research Institute, Daejeon, Republic of Korea. He is currently a professor in the Department of Cogno-Mechatronics

Engineering, Pusan National University. His present research interests include imprinted optical devices, nanophotonics, optical interconnection, and optical components for in-vehicle networks.



Chang-Seok Kim received his BS degree from Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea, in 1996; the MS degree from Gwangju Institute of Science and Technology, Gwangju, in 1999; and the PhD degree from Johns Hopkins University, Baltimore, Maryland, in 2004. From 1999 to 2000, he was a research engineer with the Wavelength Division Multiplexing Optical Communication Team